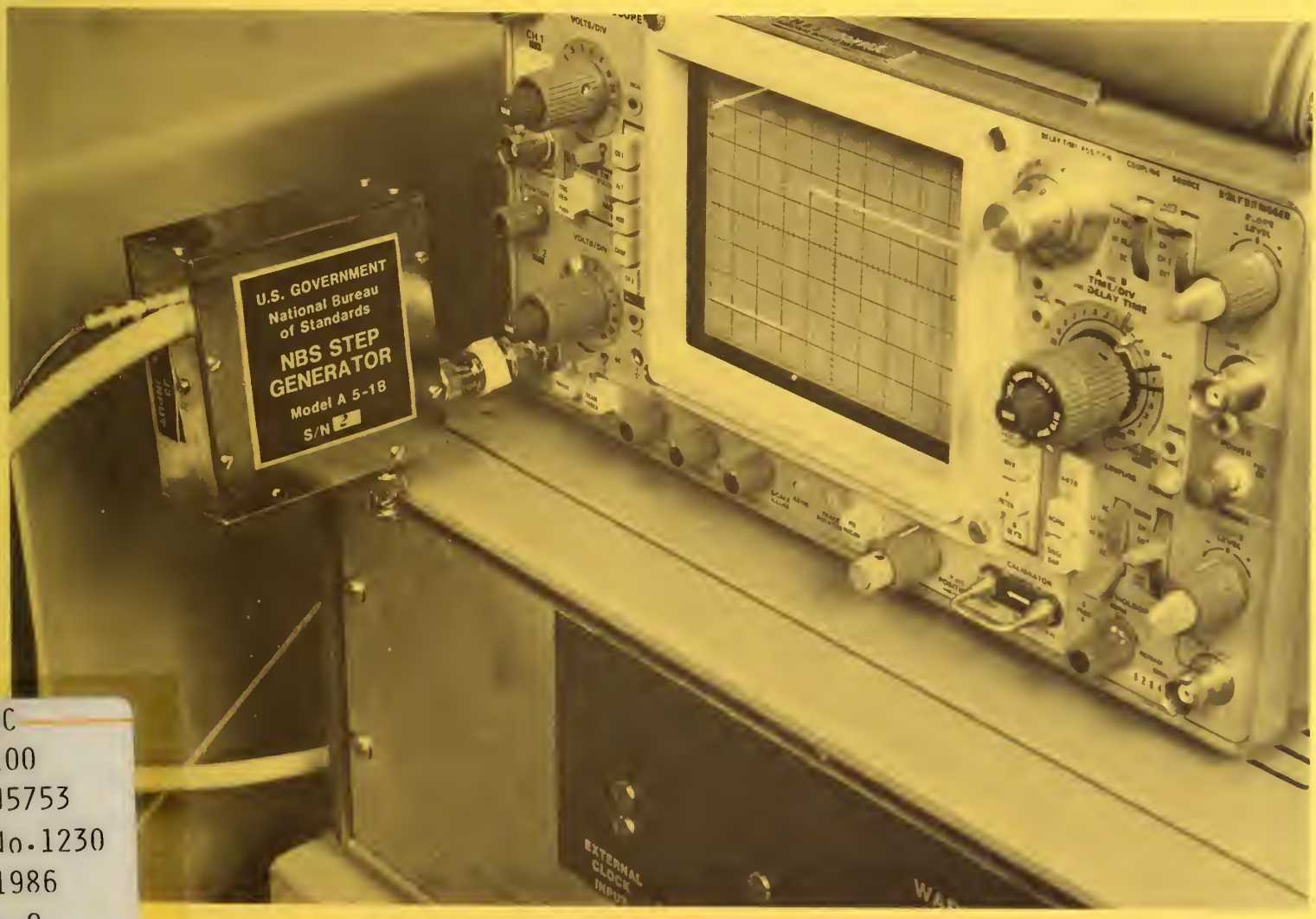
U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards

NBS Technical Note 1230

A Precision Programmable Step Generator for Use in Automated Test Systems

H. K. Schoenwetter, D. R. Flach, T. M. Souders, and B. A. Bell



The National Bureau of Standards[1] was established by an act of Congress on March 3, 1901. The Bureau's overall goal is to strengthen and advance the nation's science and technology and facilitate their effective application for public benefit. To this end, the Bureau conducts research and provides: (1) a basis for the nation's physical measurement system, (2) scientific and technological services for industry and government, (3) a technical basis for equity in trade, and (4) technical services to promote public safety. The Bureau's technical work is performed by the National Measurement Laboratory, the National Engineering Laboratory, the Institute for Computer Sciences and Technology, and the Institute for Materials Science and Engineering.

The National Measurement Laboratory

Provides the national system of physical and chemical measurement; coordinates the system with measurement systems of other nations and furnishes essential services leading to accurate and uniform physical and chemical measurement throughout the Nation's scientific community, industry, and commerce; provides advisory and research services to other Government agencies; conducts physical and chemical research; develops, produces, and distributes Standard Reference Materials; and provides calibration services. The Laboratory consists of the following centers:

- Basic Standards[2]
- Radiation Research
- Chemical Physics
- Analytical Chemistry

The National Engineering Laboratory

Provides technology and technical services to the public and private sectors to address national needs and to solve national problems; conducts research in engineering and applied science in support of these efforts; builds and maintains competence in the necessary disciplines required to carry out this research and technical service; develops engineering data and measurement capabilities; provides engineering measurement traceability services; develops test methods and proposes engineering standards and code changes; develops and proposes new engineering practices; and develops and improves mechanisms to transfer results of its research to the ultimate user. The Laboratory consists of the following centers:

- Applied Mathematics
- Electronics and Electrical Engineering[2]
- Manufacturing Engineering
- Building Technology
- Fire Research
- Chemical Engineering[2]

The Institute for Computer Sciences and Technology

Conducts research and provides scientific and technical services to aid Federal agencies in the selection, acquisition, application, and use of computer technology to improve effectiveness and economy in Government operations in accordance with Public Law 89-306 (40 U.S.C. 759), relevant Executive Orders, and other directives; carries out this mission by managing the Federal Information Processing Standards Program, developing Federal ADP standards guidelines, and managing Federal participation in ADP voluntary standardization activities; provides scientific and technological advisory services and assistance to Federal agencies; and provides the technical foundation for computer-related policies of the Federal Government. The Institute consists of the following centers:

- Programming Science and Technology
- Computer Systems Engineering

The Institute for Materials Science and Engineering

Conducts research and provides measurements, data, standards, reference materials, quantitative understanding and other technical information fundamental to the processing, structure, properties and performance of materials; addresses the scientific basis for new advanced materials technologies; plans research around cross-country scientific themes such as nondestructive evaluation and phase diagram development; oversees Bureau-wide technical programs in nuclear reactor radiation research and nondestructive evaluation; and broadly disseminates generic technical information resulting from its programs. The Institute consists of the following Divisions:

- Ceramics
- Fracture and Deformation [3]
- Polymers
- Metallurgy
- Reactor Radiation

[1] Headquarters and Laboratories at Gaithersburg, MD, unless otherwise noted; mailing address Gaithersburg, MD 20899.
[2] Some divisions within the center are located at Boulder, CO 80303.
[3] Located at Boulder, CO, with some elements at Gaithersburg, MD.

NBS Technical Note 1230

A Precision Programmable Step Generator for Use in Automated Test Systems

H. K. Schoenwetter, D. R. Flach, T. M. Souders, and B. A. Bell

Electrosystems Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Gaithersburg, MD 20899

Sponsored in part by:
Sandia National Laboratories
Albuquerque, NM 87185

December 1986

U.S. Department of Commerce
Malcolm Baldrige, Secretary

National Bureau of Standards
Ernest Ambler, Director

National Bureau of Standards Technical Note 1230
Natl. Bur. Stand. (U.S.), Tech. Note 1230, 104 pages (Dec. 1986)
CODEN: NBTNAE

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1986

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington DC 20402

TABLE OF CONTENTS

TABLE OF CONTENTS (cont.)

LIST OF FIGURES

LIST OF FIGURES (cont.)

LIST OF TABLES

A PRECISION PROGRAMMABLE STEP GENERATOR FOR USE IN AUTOMATED TEST SYSTEMS

H. K. Schoenwetter, D. R. Flach, T. M. Souders, and B. A. Bell

ABSTRACT

A precision voltage step generator has been designed for use in automated systems to test the dynamic response of waveform recorders and other instruments. The programmable pulse parameters include transition polarity, pulse length, and repetition rate. The initial and final levels of voltage steps are each programmable within the range of ± 1 V for a 50 Ω termination and within ± 5 V for a high impedance load. Voltage steps within these ranges settle to within ± 0.02% of full scale range (FSR) in less than 22 and 26 ns, respectively, for small load capacitance. The corresponding transition durations are approximately 6 and 7 ns.

1. INTRODUCTION

The NBS Step Generator was designed for use in automated test systems to characterize the transient response of waveform recorders, oscilloscopes, and other instruments.[1] In particular, the system was intended for testing waveform recorders and digitizing oscilloscopes with resolutions of 8 to 10 bits and bandwidths up to 50 MHz. The step generator system has been used to test a wide range of high performance waveform recorders. Tests were made on these units to determine: static errors, including offset, gain, linearity, and noise; transfer functions, including step response, impulse response, and frequency response; and transient errors, including dynamic linearity, settling time, transition duration, and transient thermal errors. Several of these test methods are described in a previous paper [1][2], which is reproduced in Appendix A.

The step generator was designed to output programmable voltage pulses, with one well-defined transition per period, the beginning and terminating levels of which are designated V_1 and V_2. (The transition from V_2 to V_1 is less well characterized, and is not relied upon for most measurements.) Either single shot or repetitive pulses can be generated, with the repetition rate and duty cycle programmable over many orders of magnitude. The initial and final levels defining the steps are each programmable within the range of ± 1 V for a 50 Ω termination and within ± 5 V for a high impedance load. Voltage steps within these ranges settle smoothly, with no overshoot, to within 0.1% of full scale range in less than 15 and 19 ns, respectively, for small load capacitance. The corresponding 10-90 percent transition durations are approximately 6 and 7 ns. The voltage step waveform has been characterized by independent means, and has been shown to approximate an

---

[1] NBS received the IR-100 Award for this system, which was selected by the Research and Development Magazine as one of the 100 most significant new products of 1986.

[2] Numbers in brackets refer to the literature references listed on p. 53 of this report.

exponential response. At high values of output capacitance, the more slowly rising waveform becomes sufficiently close to an exponential that it can be used for dynamic measurements of linearity errors. Since the information yielded from these measurements is important for characterizing a waveform recorder, these tests are routinely performed using two capacitance fixtures (small modules) supplied with the system.

2. THEORY OF OPERATION

2.1 Step Generator Requirements

A step generator (SG) design was sought for use in automatic test systems to characterize waveform recorders with resolutions up to 10 bits and bandwidths up to 50 MHz (rise time of 7 ns for a 6 dB/octave response roll-off). Commercial pulse generators are not accurate enough for these tests, and laboratory step generator designs lack the overall test capability required, including wide-range programmability of the pulse parameters. An earlier NBS design had an accuracy that approached the required performance [3,7], as described in the next section. The minimum SG requirements for comprehensive and accurate testing of these waveform recorders follows.

(1) The initial level, V_1, and the final level, V_2, of voltage transitions should be independently adjustable, and each should have a range of at least $\pm$ 5 V for high impedance loads. The corresponding range for 50 Ω loads should be $\pm$ 1 V. These levels should be accurately related to measurable dc values for accurate calibration.

(2) The transition duration (10-90% rise time, T_R) of the voltage steps should be less than 7 ns.

(3) The voltage step should settle to within $\pm$ 0.1% and $\pm$ 0.02% of V_2 in less than 22 ns and 27 ns, respectively, measured from the 10% amplitude point.

(4) The output impedance of the SG should be essentially resistive for frequencies ranging from dc to several times the upper cutoff (- 3 dB) frequency of the test instrument. A passive output circuit is preferred.

(5) The SG output circuit should be packaged for direct connection to the test device, to avoid losses (and pulse distortion) from a connecting cable.

(6) The pulse width and pulse repetition rate should be independently selectable, with pulse widths ranging from 50 ns to 5 ms, and repetition rates up to 5 MHz. After settling to level V_2 with $\pm$ 0.02% accuracy, the voltage must remain within these error bounds for all pulse widths.

(7) All pulse parameters should be programmable, so that the SG may be used in automatic test systems.

A practical level of accuracy for a settled voltage step is ~1/2 LSB of the waveform recorder under test. Thus, in item 1, if the static accuracy of V_2 is $\pm$ 0.03%, the settling error (item 3) should be no more than $\pm$ 0.02% for a 10-bit recorder. For an 8-bit recorder, the allowable settling error could be as large as $\pm$ 0.17%, etc. The accuracy of V_1 should be at least $\pm$ 2%.

The rise and settling times given in (2) and (3) are minimum requirements for the application. Smaller values would simplify the error analysis of the test recorders.

Item 4 is desired so that overshoot and ringing in the voltage step are minimal if the input circuit of the test instrument has significant parasitic reactances (lead inductance and shunt capacitance, etc.)

Item 5 is very important, since a terminated connecting cable greatly increases the settling time (ST). When an unterminated cable is used, cable capacitance or voltage reflections may increase the ST. The effects of a connecting cable on ST are discussed in [2].

In item 6, pulse widths of several milliseconds are desirable for measuring thermal transients in the test instruments.

2.2 Design Approaches

2.2.1 Prior Techniques

In previous years, tunnel diodes and mercury relays have been employed in SGs to yield rise times as low as 20 ps and 39 ps, respectively [3]. However, these SGs had poor settling characteristics, i.e., the uncertainty of the voltage after transitions was 1 to 2 percent, or larger [4, 5].

In an effort to obtain step-like waveforms of known amplitude and flatness, a number of SGs or waveform standards have been developed at NBS, using various techniques. For example, reference 6 describes the development of a solid-state waveshaping filter that yields a 1/4 V step with a transition duration of 400 ps, when the filter is excited by a tunnel diode SG. The output waveform of the filter has a smooth transition with negligible aberrations; however, ST information is not available.

The reference flat pulse generator (RFPG) described in [3] and [7] has the following important characteristics[3]: (1) the initial and final voltage levels of the transitions are calibrated from dc measurement; (2) the transition duration of the voltage steps is very small; and (3) the output voltage is flat after settling. This SG employs very fast precision Schottky diode switching circuits to obtain an output step of $\pm$ 0.50 V to 0.00 V.

The basic RFPG circuit is shown functionally in figure 2.1. Current I_1 flows through diode D2 and the 25 Ω parallel resistance of R_g and load resistance R_L; thus, $V_o(t) = 0.5$ V. When the control pulse is applied, switch S changes from position 1 to position 2. Diode D1 conducts 10 mA for a nodal current balance and D2 is reverse biased and becomes nonconducting. Therefore, $V_o(t)$ rapidly approaches 0 V. In practice, the current switching by S is performed by an NPN emitter-coupled differential switch pair, and I_1 and I_2 are current sources employing PNP and NPN transistors, respectively.

---

[3] These papers also briefly describe or reference other pulse generators or waveform standards that have been developed for testing high-speed instruments.

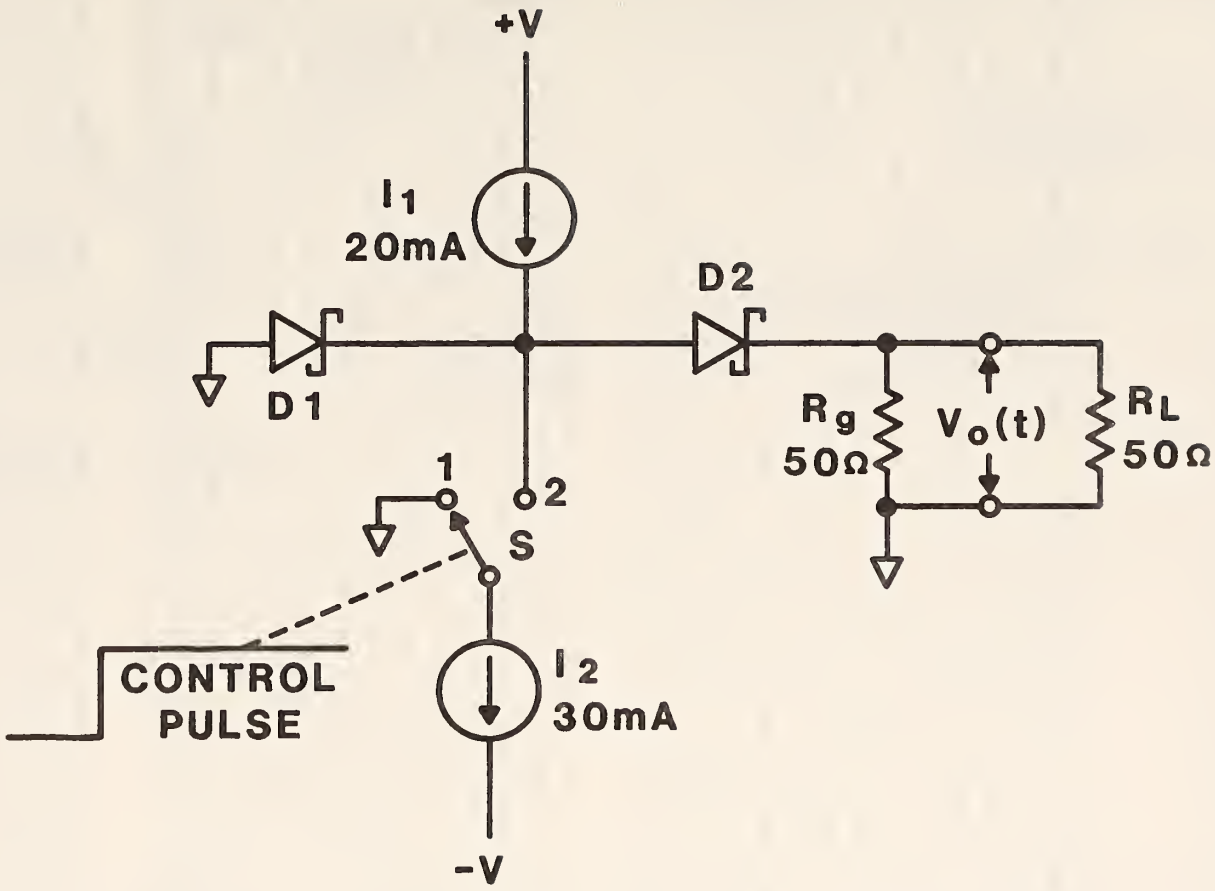


Fig. 2.1 Functional diagram of the NBS reference flat pulse generator (RFPG).

The baseline of the output step differs from 0 V by less than 10 μV, and the top line equals 0.5 V ± 0.1%, assuming $R_L = R_g$.

The measured transition duration of this generator is 600 ps, and the measured ST to ± 0.2% accuracy is approximately 8 ns. ST measurements to better than 0.2% were not available for this instrument. However, the RFPG was not specifically designed for settling accuracies better than 1%. The RFPG has other limitations which reduce its suitability for the applications considered here. These include inadequate step size, and the inability to select other initial and final step voltages.

2.2.2 Present Design

Figure 2.2 is a functional diagram of the SG that was designed to meet the preceeding specifications [8]. Two output ranges are provided: a ± 5 V range from output H, intended for high-impedance loads, and a ± 1 V range from output L for 50 Ω loads. Operation is as follows: the voltage-to-current converter linearly converts programmable voltage V_B to current I over the range of ± 80 mA. When the TTL input is HIGH, current I is steered to output 2 of switch S. Output voltage V_H is determined by the programmable voltage V_A and the ratio (R2 + R3)/(R1 + R2 + R3) formed by the resistive voltage divider. Hence, $V_H = V_A/2$. When the TTL input is LOW, current I is steered to output 1 of S, changing V_H by IR_p, where R_p is the parallel resistance of R1 and (R2 + R3). Thus, $V_H = V_A/2 + IR_p$. Resistance R_p, equal to 125 Ω, is also the source impedance for V_H. The low-level output V_L is equal to $V_H/5$. When output L is used, the 50 Ω terminating resistor R3 shown in figure 2.2 is actually the input impedance of the test device; otherwise a 50 Ω coaxial termination is used.

Switch S operates within a few nanoseconds after the TTL input changes state. Also, when it switches current I from terminal 1 to terminal 2, all active elements are isolated from terminal 1. Consequently, the transition from $(V_A/2 + IR_p)$ to $V_A/2$, is an exponential waveform determined by R_p and the total capacitance between terminal 1 and ground. Since the transition to $V_A/2$ involves only passive elements, it can be much more accurately characterized than the reverse transition, which involves active elements. Therefore, the transition to $V_A/2$ is recommended for waveform recorder testing. The initial and final levels of this transition have been designated V_1 and V_2. Output voltage $V_L(t)$ has a smaller settling time than $V_H(t)$, but has essentially the same waveshape. The pulsewidth and repetition rate are determined by the timing circuit, which is under computer control, as are programmable voltage supplies A and B, via the IEEE-488 bus. In practice, the timing circuit is a programmable pulse generator with TTL-type output pulses.

Since rapid load current changes cause output voltage transients in most voltage supplies, dummy load R4-R5 and complementary switching circuits in current switch S and the voltage-to-current converter are employed to maintain constant load currents for voltage supplies A and B. Also, terminal 3, placed physically close to R1, is carefully bypassed so that the impedance to ground is essentially zero for the frequency range of interest. In order to enhance the effective accuracies of V_H and V_L, corrections to the resistance ratios and values of V_A can be stored in a computer for later application to test data. Since the relative heat dissipation in R1 and (R2 + R3) varies with changes in V_A, I, and pulse duty cycle, resistors R1 and R2 (metal film) were chosen to have small temperature coefficients.

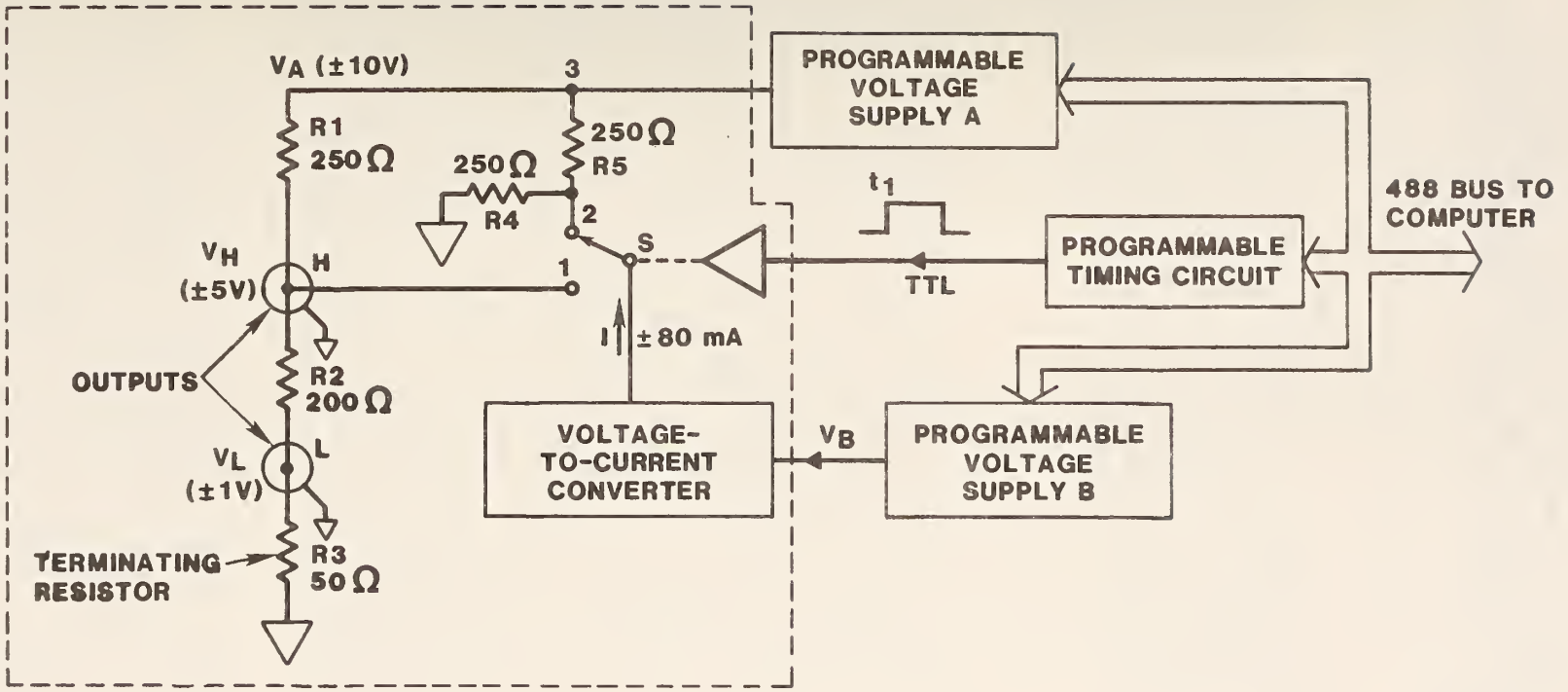


Fig. 2.2 Precision step generator. The pulse level following a voltage step transition is determined by V_A. Amplitude and polarity of the transition are determined by current I, which is a linear function of V_B. Voltage ranges are $\pm$ 5 and $\pm$ 1 V from outputs H and L, respectively. Pulse width and repetition rate are determined by the TTL input from the timing circuit.

The circuits shown in the dotted outline comprise the output circuit of the SG, and are contained in a small package ("test head") which may be connected directly to the instrument under test. The programmable voltage supplies and timing circuit are contained in a separate support package, which is designated the control unit.

3. GENERAL DESCRIPTION OF SYSTEM

The NBS Step Generator (SG) is designed to output programmable voltage pulses, with one well-defined transition per period, the beginning and terminating levels of which are designated V_1 and V_2. The SG consists of the output circuit and the control unit, which were described briefly in section 2.2.2. As mentioned previously, the system also includes two capacitance modules for dynamic linearity measurements.

Figure 3.1 shows the SG in an automated test system. Overall control is provided via the IEEE-488 bus, for which an internal interface (not shown) has been provided. The waveform recorder under test is also interfaced to the controller via this bus. The output circuit of the step generator is a small test head which connects directly to the input terminal of the waveform recorder under test. The control unit provides the power, precision dc voltage levels (V_A, V_B), polarity selection pulses, and timing pulses necessary to control the parameters of the voltage steps generated in the output circuit.

3.1 Output Circuit

The step generator output circuit, shown in figure 3.2 is packaged in a small, lightweight container that is separate from the voltage supplies and timing circuit. Output connectors H and L are male BNC connectors which permit direct connection to a waveform recorder, or other measuring device, without the use of a coaxial cable. The step generator actually consists of two, essentially complementary, voltage step generators-one for each polarity of transition. A simplified schematic diagram of the circuit used for producing positive voltage steps is shown in figure 3.3. Transistors Q1 and Q2 perform the function of switch S in figure 3.2, switching current I to terminal 1 or I' to terminal 2. Collector currents I and I' are proportional to the common base current gains of Q1 and Q2, and typically differ by less than two percent. The magnitude of I is approximately $(|V_B|-8.3)/125$. (Example: for a 6V step at connector H, I = 48 mA and $|V_B| = 14.3$V). Schottky TTL buffers U1 and U2 provide the drive currents for Q3 and Q4, which alternately bias Q1 and Q2 off. Operation is as follows: prior to the TTL input pulse, the outputs of U1 and U2 are LOW and HIGH, respectively, so that Q3 is biased off and Q4 is conducting. Therefore, Q2 is biased off and Q1 conducts current I to terminal H, yielding an output voltage $V_H = V_A/2+IR_p$. Upon application of the TTL pulse at time T_1, the outputs of U1 and U2 switch to HIGH and LOW levels, respectively, switching Q3 on and Q4 off. This action switches Q1 off and Q2 on. Consequently, voltage V_H switches to level $V_A/2$.

Except for some modification of the TTL buffer circuits and the biasing of the lower pair of transistors, the circuit for producing negative voltage steps is essentially the complement of the circuit shown in figure 3.3. A latching DPDT relay is employed to connect Q1 or its complementary counterpart to connector H or to ground. A second DPDT relay is used to apply $\pm$ 5 V to Q3, Q4, U1, U2, or their counterparts. Thus, programming the SG includes pulsing the appropriate relay windings to select the voltage step polarity. Diodes D1 and D2 protect Q1 and Q2 when these transistors are disabled.

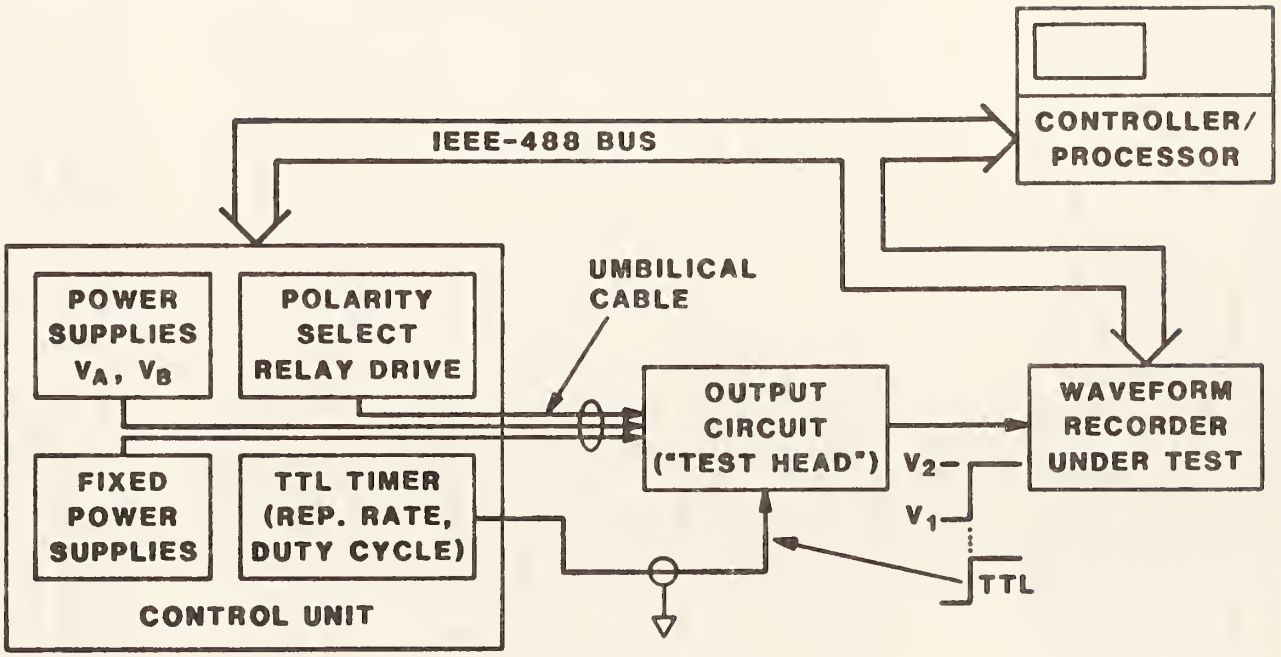


Fig. 3.1 Automated test system. The step generator consists of the control unit and the output circuit. All functions shown in the control unit are programmable via the IEEE-488 bus, except for the fixed power supplies.

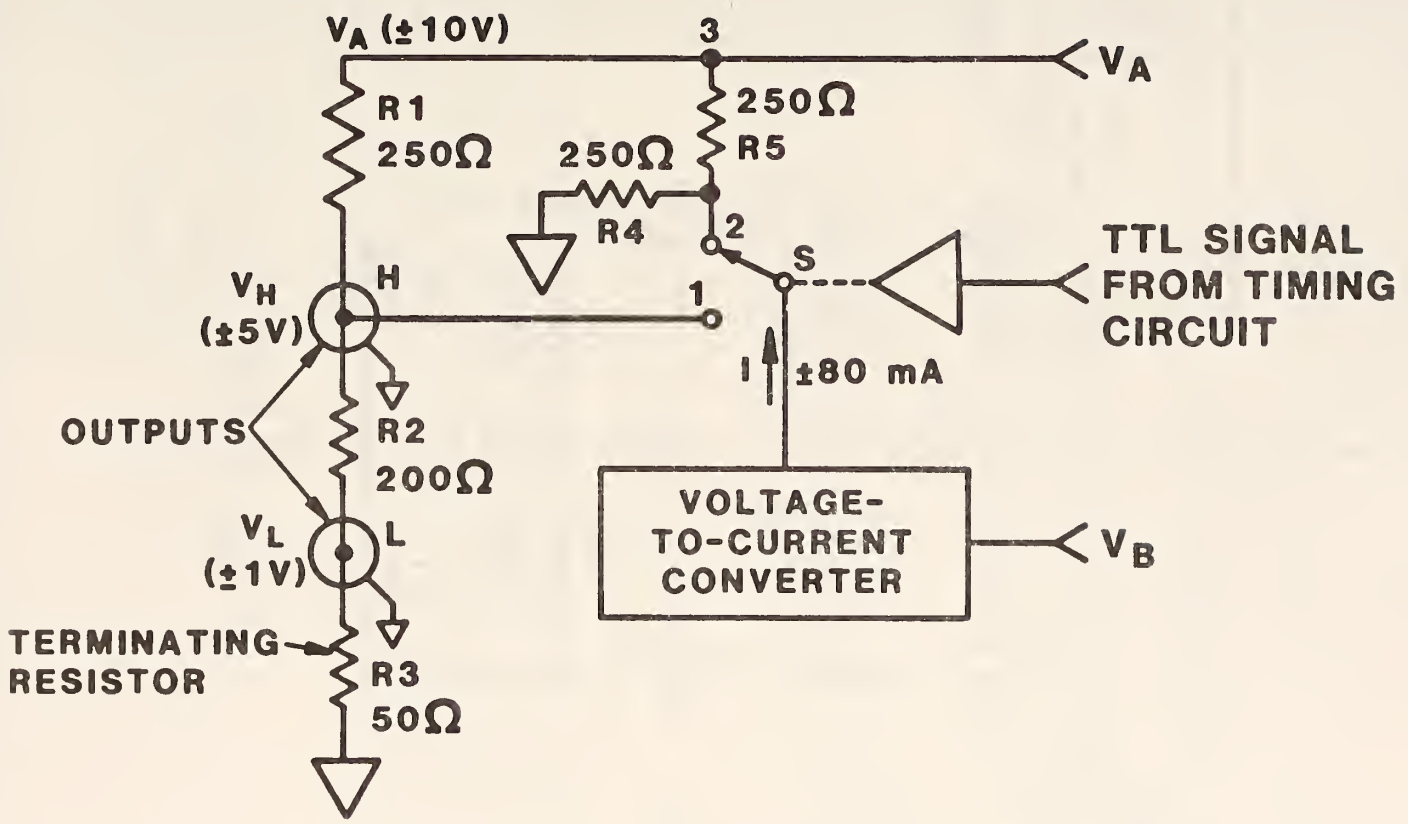


Fig. 3.2 Functional diagram of the step generator output circuit.

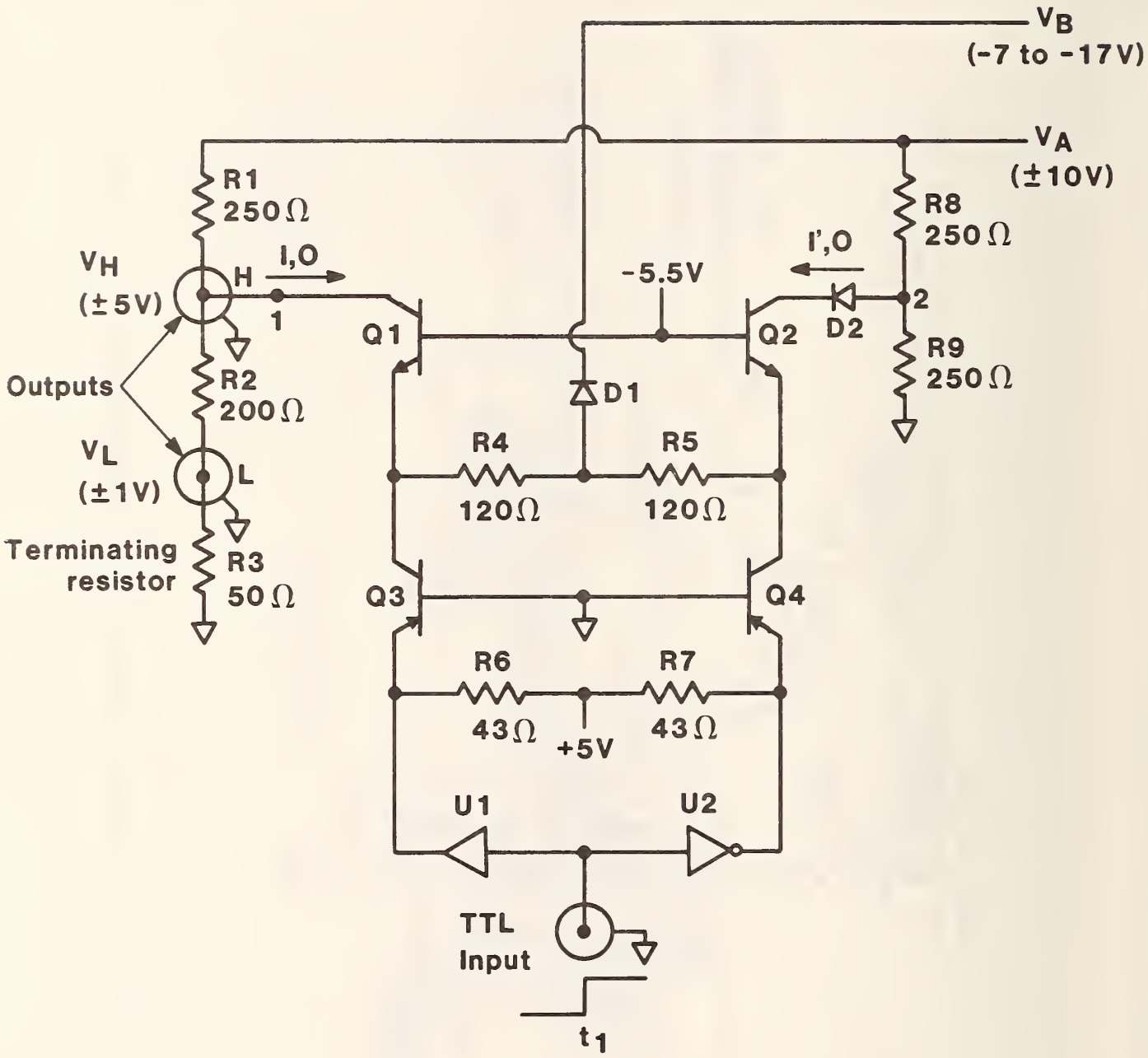


Fig. 3.3 Simplified diagram of the output circuit for producing positive voltage steps. Transistors Q1 and Q2 perform the function of switch S in figure 2.2.

A detailed diagram of the complete output circuit is shown in figure 3.4. The circuits for producing negative and positive voltage steps are shown on the left and right sides of the drawing, respectively. The functions of some of the components/circuits not shown in figure 3.3 are given below:

(1) Clipping diodes CR4-CR9 and CR15-CR20 are used to keep transistor pairs Q3, Q4, and Q7, Q8 out of saturation, respectively. Preventing saturation permits pulse repetition rates up to 10 MHz.

(2) Diodes CR2, CR3, and CR13, CR14 minimize switching transients, capacitively coupled to the collector circuits of Q1 and Q5, respectively.

(3) R40 and R41 are selected for minimum settling time for negative and positive transitions, respectively.

(4) Capacitors C30-C41 were added to minimize the effect of capacitive loading of voltage supply V_A, when large capacitors are connected across output H for dynamic linearity tests (discussed later).

The numbered leads, ranging from 1 to 18, refer to umbilical connector pin numbers.

Figure 3.5 is a photograph showing connector L ($\pm$ 1 V range) of the output circuit connected to an oscilloscope. Since the oscilloscope has a high input impedance, a 50 ohm coaxial termination is required. The output circuit test head dimensions are approximately 7.6 x 7.6 x 3.8 cm, excluding connectors, and its weight is approximately 200 g.

3.2 Control Unit

3.2.1 General Description

Figure 3.6 shows a complete block diagram of the control unit. Overall control is provided via the IEEE-488 bus for which an internal listener interface has been provided. This bus interface, in turn, drives a system bus to distribute data for controlling the operating parameters of the step generator output circuit (test head). These parameters are: the pulse repetition rate, pulse length, voltage step polarity, and the initial and final voltage levels (V_1, V_2, respectively) of the step. The ranges of the pulse parameters are as follows:

- Pulse repetition rate: 153 Hz to 5 MHz
- Pulse length: 20 ns to ~ 6 ms
- Duty cycle: approximately 5% to 95%
- V_1, V_2: $\pm$ 5 V
- Polarity of transition: either + or -

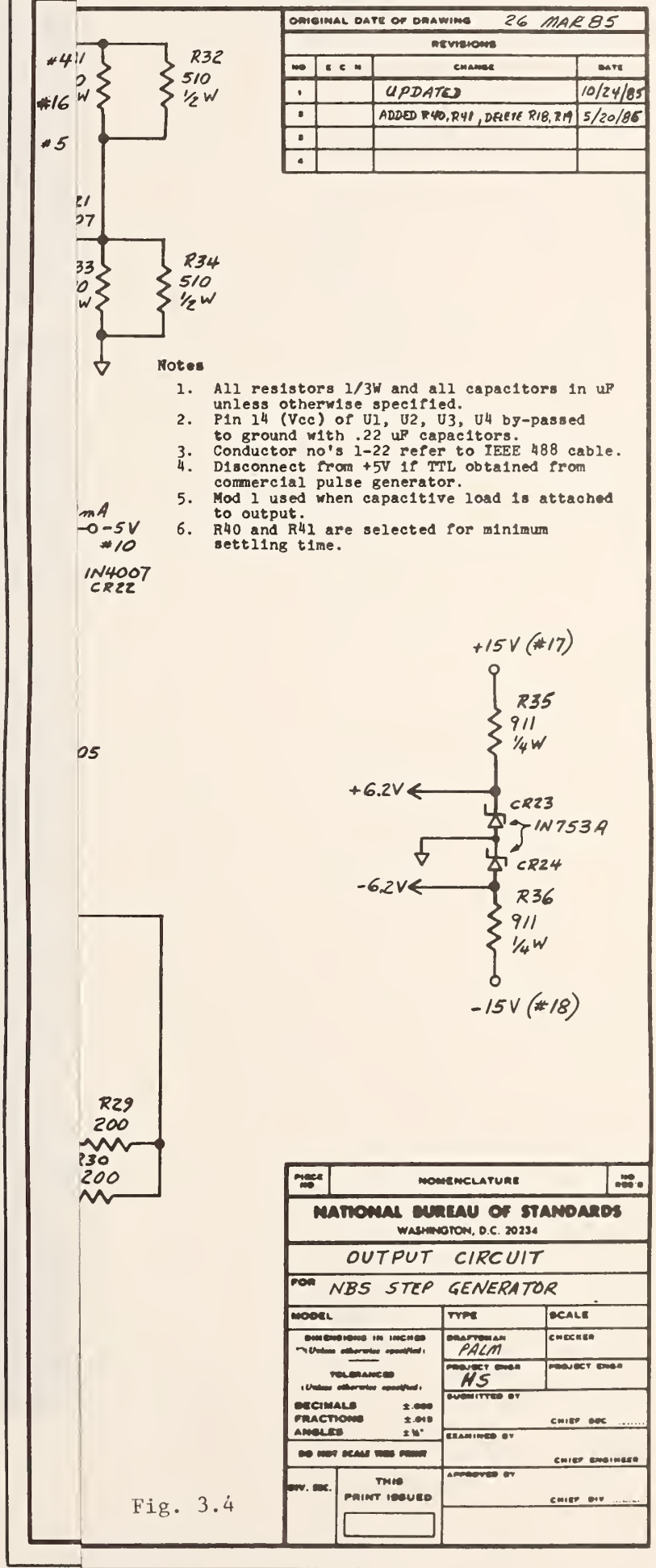
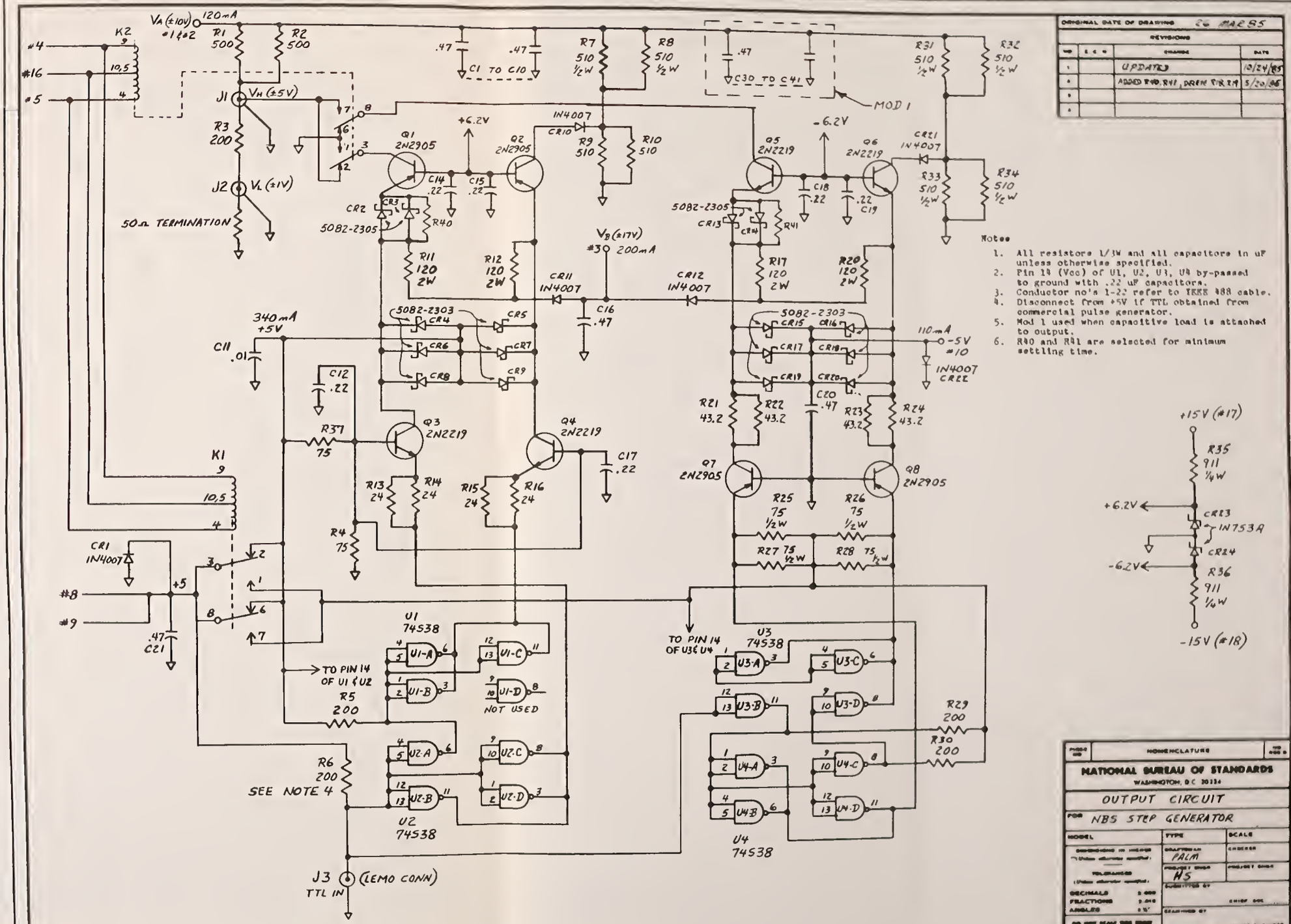

ORIGINAL DATE OF DRAWING 26 MAR 85
REVISIONS
NO | E C N | CHANGE | DATE
1 | | UPDATED | 10/24/85
2 | | ADDED R40, R41, DELETE R18, R19 | 5/20/86
3 | | |
4 | | |
#411
#16
#5
R32
510
½W
R34
510
½W
Notes
1. All resistors 1/3W and all capacitors in uF unless otherwise specified.
2. Pin 14 (Vcc) of U1, U2, U3, U4 by-passed to ground with .22 uF capacitors.
3. Conductor no's 1-22 refer to IEEE 488 cable.
4. Disconnect from +5V if TTL obtained from commercial pulse generator.
5. Mod 1 used when capacitive load is attached to output.
6. R40 and R41 are selected for minimum settling time.
mA
-5V
#10
IN4007
CR22
+15V (#17)
R35
911
¼W
+6.2V
CR23
IN753A
CR24
-6.2V
R36
911
¼W
-15V (#18)
R29
200
R30
200
PIECE NO
NOMENCLATURE
NO REQ'D
NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234
OUTPUT CIRCUIT
FOR NBS STEP GENERATOR
MODEL
TYPE
SCALE
DRAFTSMAN PALM
CHECKER
PROJECT ENGR HS
PROJECT ENGR
SUBMITTED BY
CHIEF SEC
EXAMINED BY
CHIEF ENGINEER
APPROVED BY
CHIEF DIV
DIV. SEC.
THIS PRINT ISSUED

Fig. 3.4



ORIGINAL DATE OF DRAWING 26 MAR 85

NO	LTR	CHANGE	DATE
1		UPDATED	10/24/85
2		ADDED R40, R41, DRAIN R13 R14	5/20/86
3			
4			

Notes

1. All resistors 1/3W and all capacitors in uF unless otherwise specified.
2. Pin 14 (Vcc) of U1, U2, U3, U4 by-passed to ground with .22 uF capacitors.
3. Conductor no's 1-22 refer to IEEE 488 cable.
4. Disconnect from +5V if TTL obtained from commercial pulse generator.
5. Mod 1 used when capacitive load is attached to output.
6. R40 and R41 are selected for minimum settling time.

NOMENCLATURE

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

OUTPUT CIRCUIT

FOR NBS STEP GENERATOR

MODEL	TYPE	SCALE
	DRAFTSMAN PALM	ENGINEER
	PROJECT ENGR HS	PROJECT ENGR
DECIMALS ± .000 FRACTIONS ± .000 ANGLES ± 0°	SUBMITTED BY	CHIEF DIV.
DO NOT SCALE THIS PRINT	DRAWN BY	CHIEF ENGINEER
	TRACED PRINT ISSUED	APPROVED BY CHIEF DIV.

Fig. 3.4

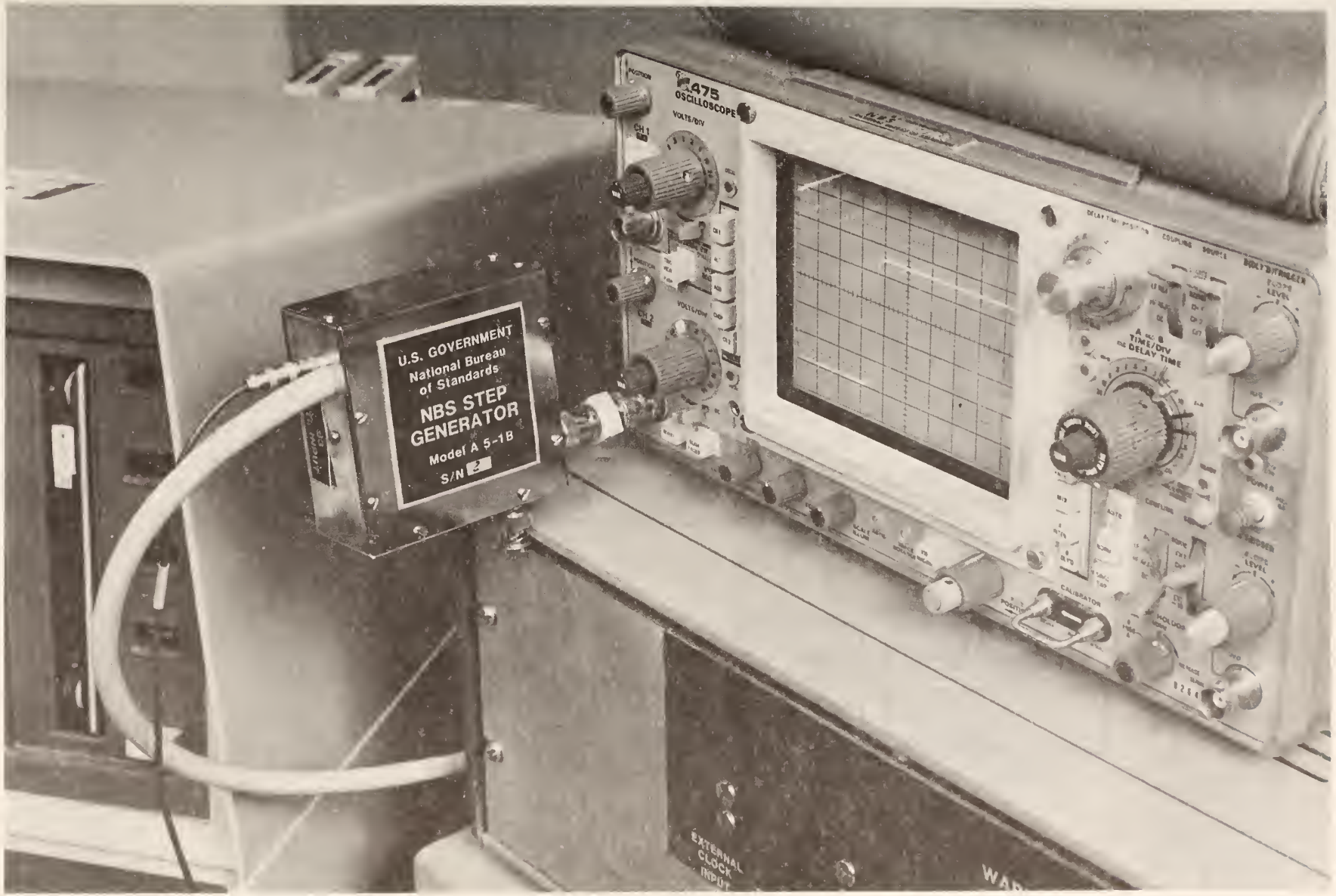


Fig. 3.5 Photograph showing the step generator output circuit connected to an oscillosope.

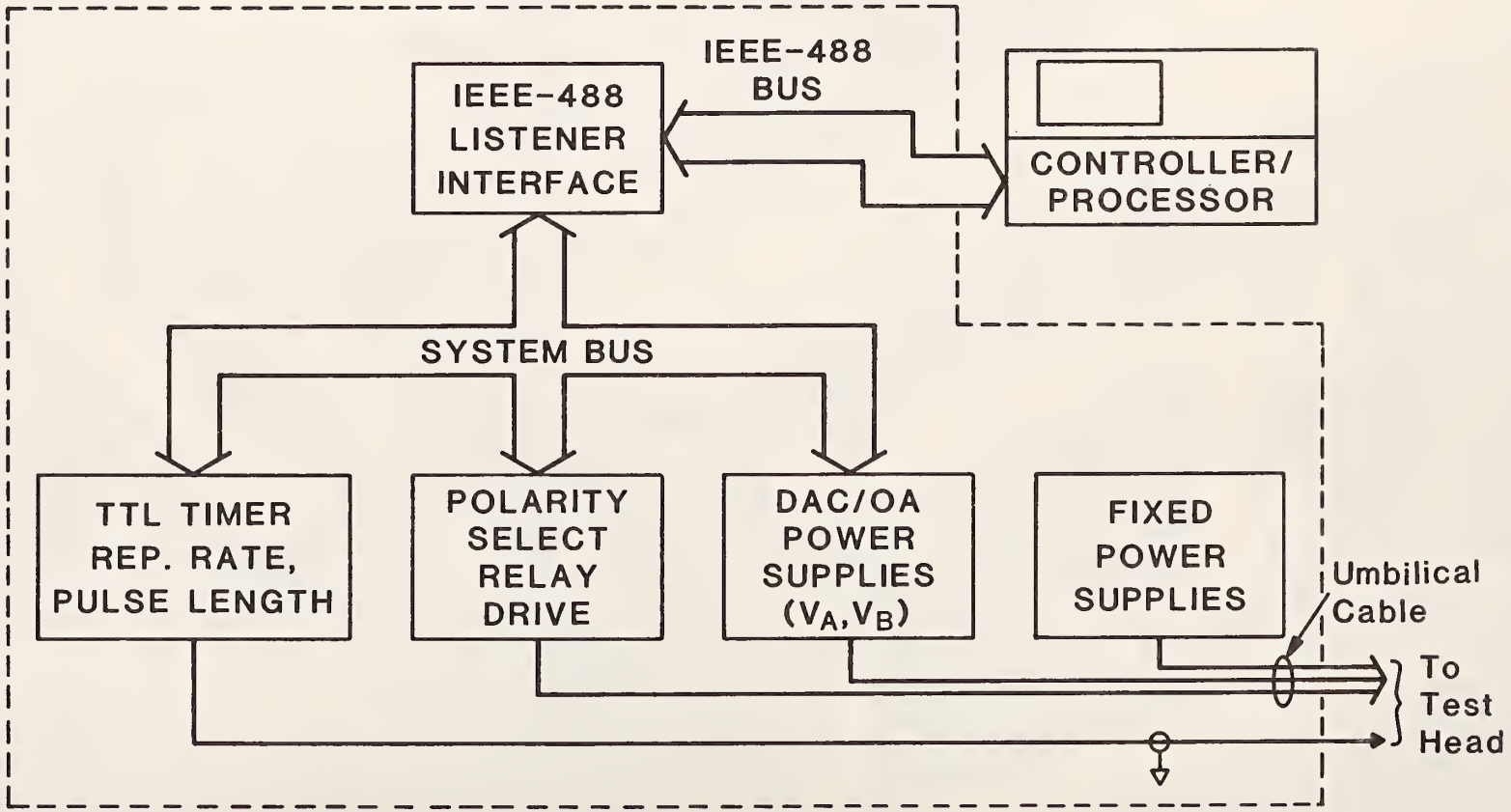


Fig. 3.6 Complete block diagram of the control unit.

The most critical of these parameters is V_2, which is equal to $V_A/2$. For a given (selected) value of V_2, V_A should be invariant over the complete ranges of the other parameters. Also, the resolutions in the selection of V_2 and V_1 are determined by the resolutions of V_A and V_B (0.024% for V_A and 0.09% for V_B). The details of the circuits that determine the pulse parameters is given in later sections. A photograph of the control unit is shown in figure 3.7.

3.2.2 Backplane Wiring

The backplane wiring and connectors for the plug-in circuit boards are shown in figure 3.8. The circuit boards and 108-pin mating connectors are numbered according to their position in the card cage (see figure 3.9). As mentioned previously, the IEEE-488 bus is connected to J8 (rear panel) of the control unit. Eight-conductor and eighteen-conductor flat cables are used to connect J8 to the connector (#3) for the IEEE-488 interface board. These pin connections are outlined by dashed lines.

It is seen that control signals from the interface board are sent only to the Timing, DAC/OA, and Output boards (boards 5, 7, and 9, respectively). The pin numbers (A6, B6, C12, etc.) to which wires are connected are used to designate the signal lines on the schematic drawings for these four boards. The regulated voltage supplies required for powering the step generator control unit and output circuit are mounted on boards 11, 15, 19, and 23. Also, the frequency synthesizer board (FREQ. SYN.) is not employed in the present application.

3.2.3 IEEE-488 Interface

A schematic diagram of the IEEE-488 interface circuit board is shown in figure 3.10. These circuits represent a hardware (chip level) implementation of an IEEE-488 interface having the following functions: acceptor handshake function, device clear function, and listener function, extended to honor secondary addresses [9]. The following sections provide a detailed description of the design of this particular implementation.

The components of the IEEE-488 bus are the data bus, the transfer bus, and the management bus. Transceiver ICs U01 and U02 interface with the data bus (signals DI01-DI08), and transceiver ICs U03 and U04 interface with the transfer and management buses.[4] The transfer bus handles handshake duties and includes the three signal lines DAV (data valid), NDAC (data not accepted), and NRFD (not ready for data). Of the five signal lines in the management bus, only the ATN (attention) and IFC (interface clear) lines are used in this application.

3.2.3.1 Purpose of Interface

Three circuit boards in the control unit are used to control the pulse parameters of the SG, and a certain amount of information must be stored on these boards to quantify these parameters. Shown in the following table are the bits of information used to quantify each parameter, the number of memory chips (ICs) used to store this information, and the circuit board location.

---

[4] These interface buffers have inverters in the input/output lines from/to the IEEE-488 bus.

Fig. 3.7 Front panel view of the control unit.

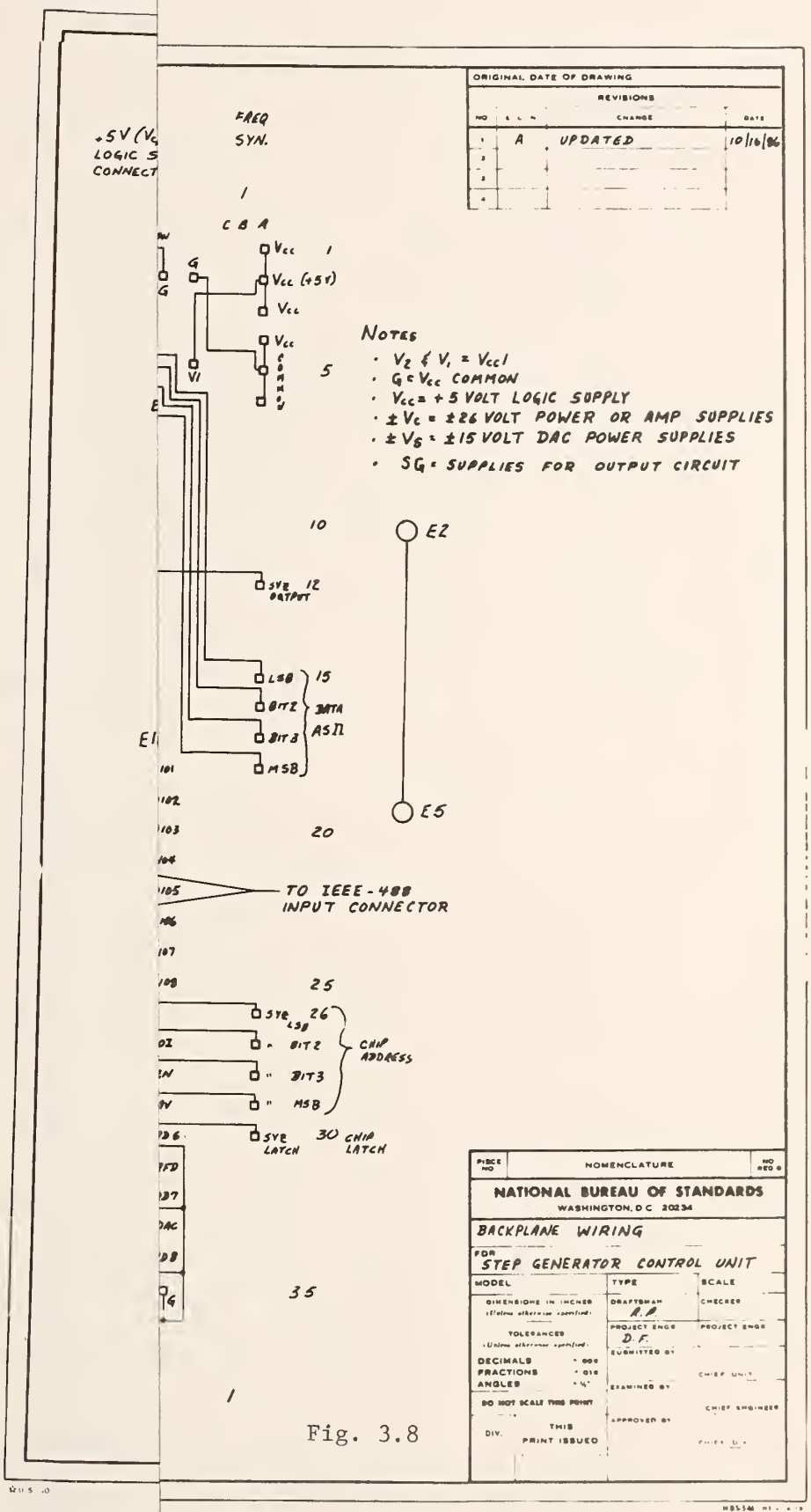

ORIGINAL DATE OF DRAWING
REVISIONS
NO
CHANGE
DATE
A
UPDATED
10/16/86
FREQ SYN.
+5V (V
LOGIC S
CONNECT
C B A
Vcc 1
Vcc (+5V)
Vcc
Vcc
COMMON
5
G
VI
NOTES
· V2 & V1 = Vcc1
· G = Vcc COMMON
· Vcc = +5 VOLT LOGIC SUPPLY
· ±Vc = ±26 VOLT POWER OR AMP SUPPLIES
· ±VG = ±15 VOLT DAC POWER SUPPLIES
· SG = SUPPLIES FOR OUTPUT CIRCUIT
10
E2
SYR OUTPUT 12
LSB 15
BIT2
BIT3
MSB
DATA ASM
E1
E5
20
TO IEEE-488 INPUT CONNECTOR
25
SYR LSB 26
BIT2
BIT3
MSB
CHIP ADDRESS
SYR LATCH 30
CHIP LATCH
35
PIECE NO
NOMENCLATURE
NO REQ'D
NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234
BACKPLANE WIRING
FOR
STEP GENERATOR CONTROL UNIT
MODEL
TYPE
SCALE
DIMENSIONS IN INCHES
(Unless otherwise specified)
DRAFTSMAN
R.P.
CHECKED
TOLERANCES
(Unless otherwise specified)
PROJECT ENGR
D.F.
PROJECT ENGR
SUBMITTED BY
DECIMALS
FRACTIONS
ANGLES
CHIEF UNIT
EXAMINED BY
DO NOT SCALE THIS PRINT
CHIEF ENGINEER
APPROVED BY
DIV.
THIS PRINT ISSUED
CHIEF D.

Fig. 3.8

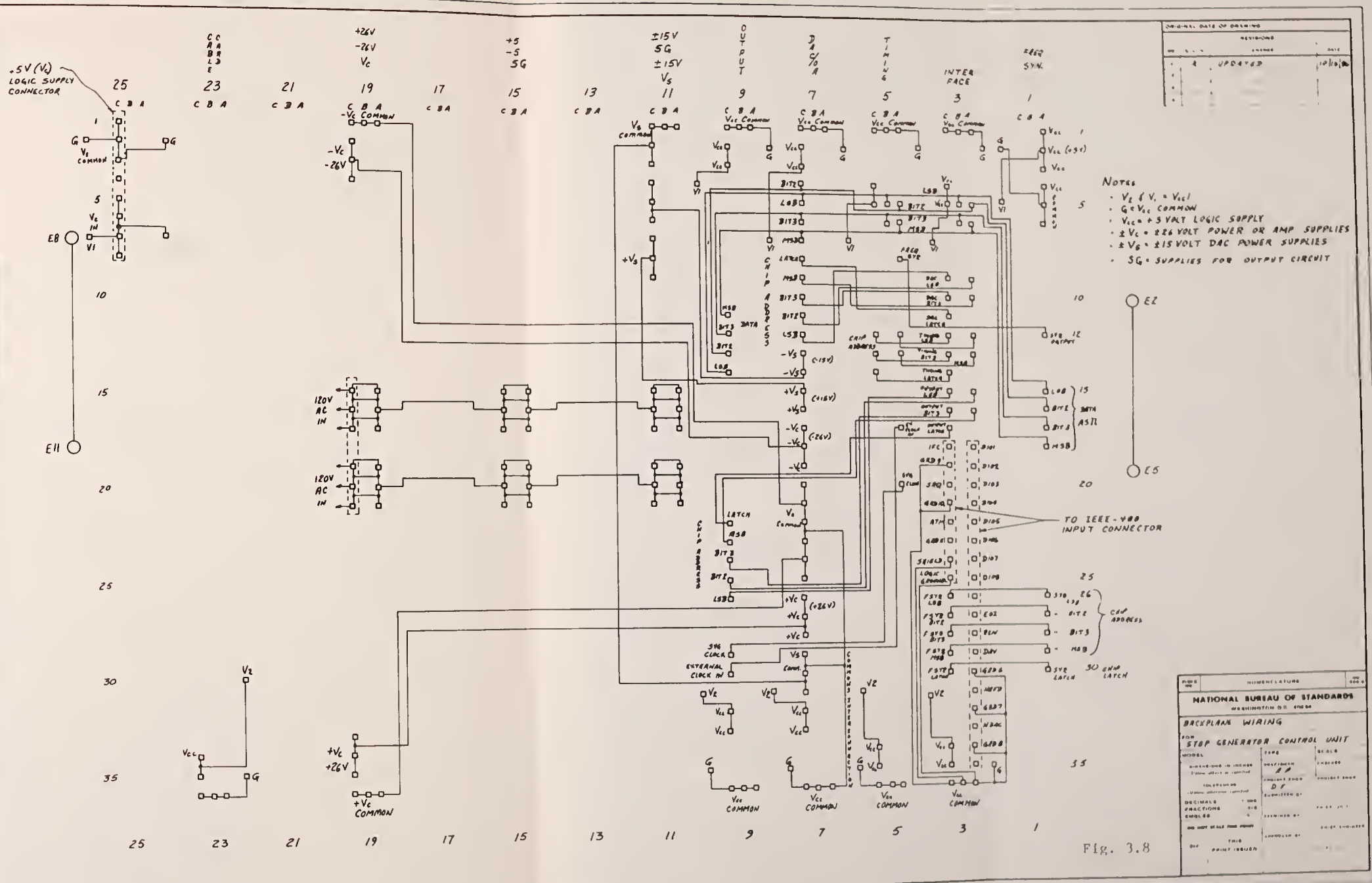
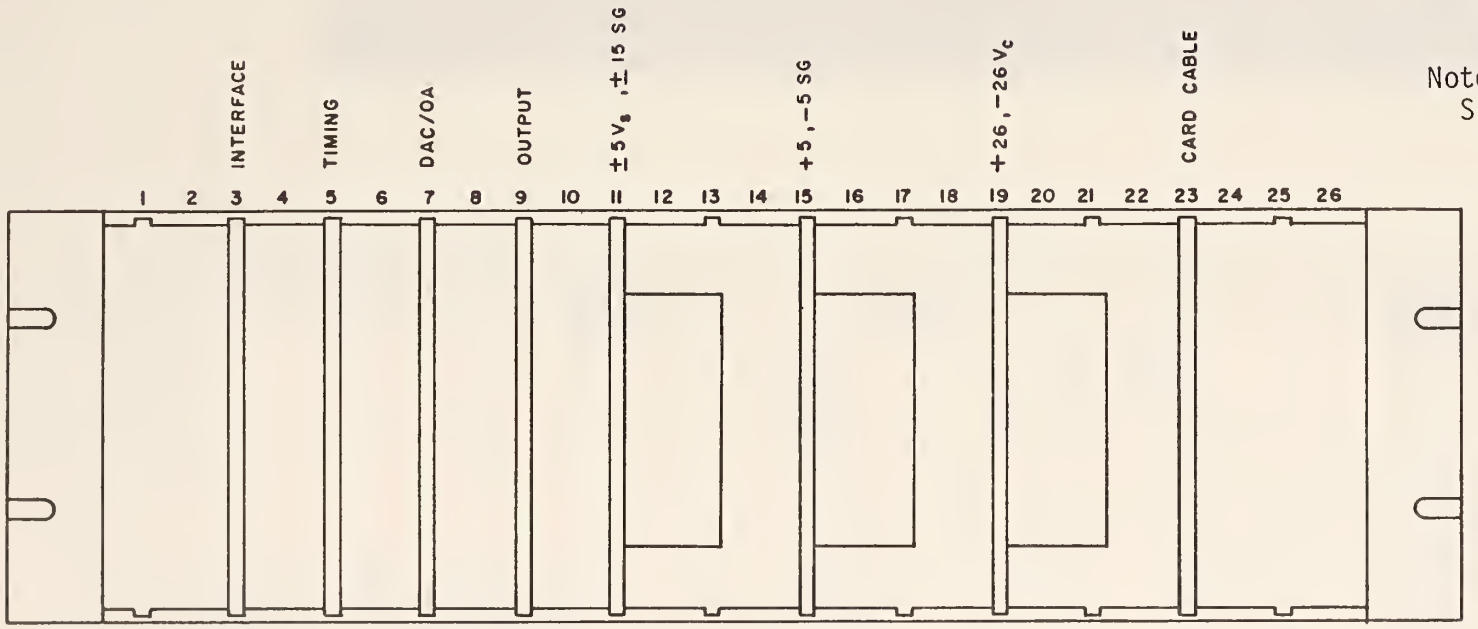

+5V (V_L) LOGIC SUPPLY CONNECTOR
CABLE
+26V
-26V
V_c
+5
-5
SG
±15V
SG
±15V
V_s
OUTPUT
D/A C/A
TIMING
INTER FACE
FREQ SYN.
NOTES
• V_L & V_{cc} = V_{cc}
• G = V_{cc} COMMON
• V_{cc} = +5 VOLT LOGIC SUPPLY
• ±V_c = ±26 VOLT POWER OR AMP SUPPLIES
• ±V_s = ±15 VOLT DAC POWER SUPPLIES
• SG = SUPPLIES FOR OUTPUT CIRCUIT
120V AC IN
120V AC IN
TO IEEE-488 INPUT CONNECTOR
EXTERNAL CLOCK IN
+Vc COMMON
NATIONAL BUREAU OF STANDARDS
BACKPLANE WIRING
FOR
STEP GENERATOR CONTROL UNIT

Fig. 3.8



Note:
SG = Supplies for Output Circuit

Fig. 3.9 Circuit board locations in the control unit.

ORIGINAL DATE OF DRAWING 10 MAR 86			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

BOARD POSITIONS

FOR
STEP GENERATOR CONTROL UNIT

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN PALM	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR D.F.	PROJECT ENGR
DECIMALS ±.008 FRACTIONS ±.016 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC.	THIS PRINT ISSUED	APPROVED BY CHIEF, DIV.

U.S. GOVERNMENT PRINTING OFFICE 1984—O-717-718

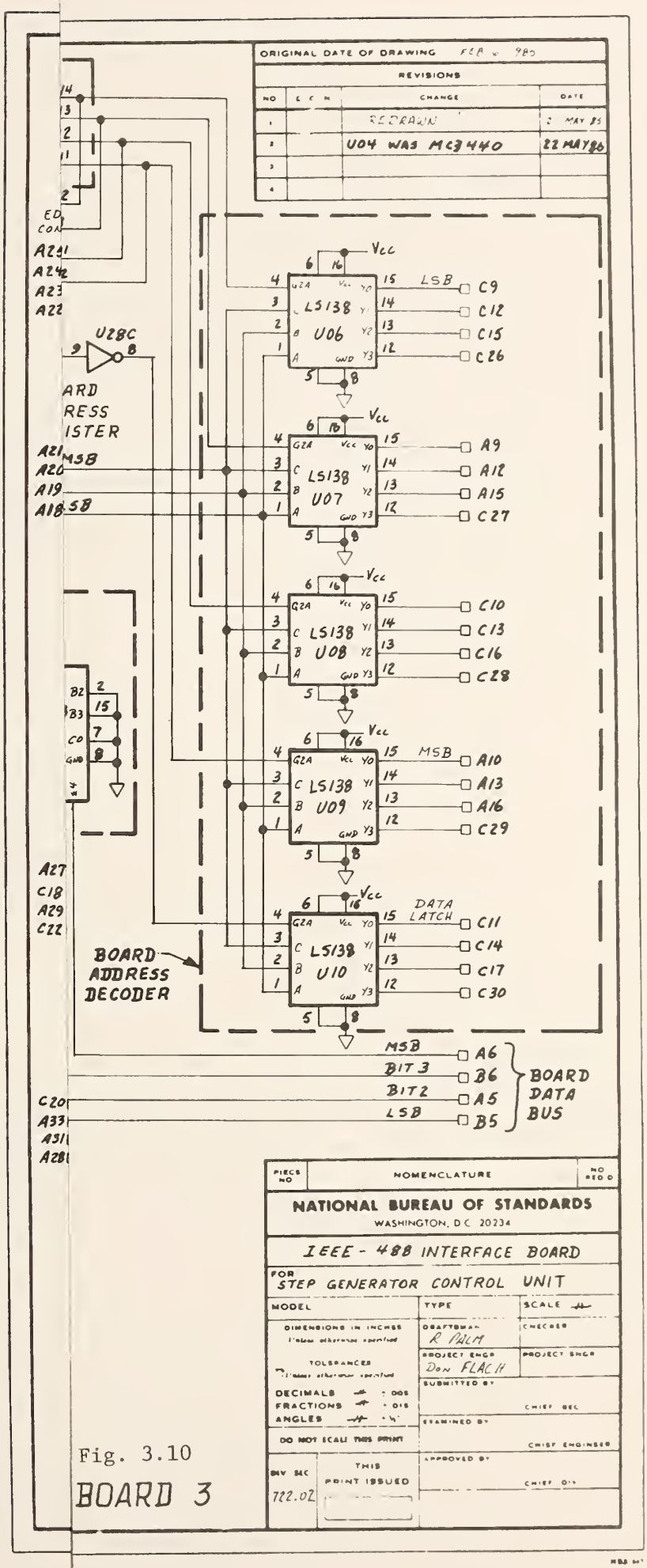


Fig. 3.10

BOARD 3

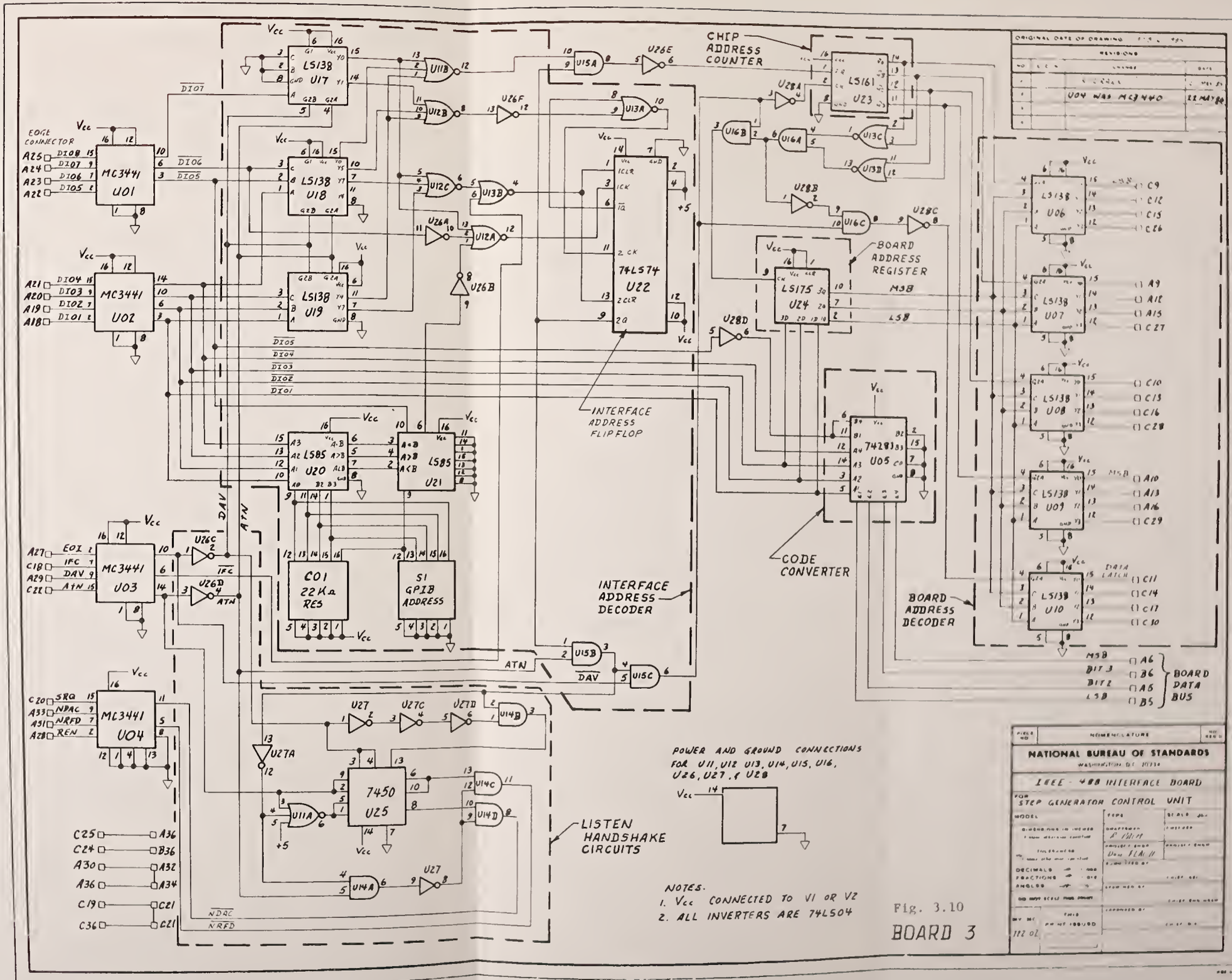

CHIP ADDRESS COUNTER
EDGE CONNECTOR
INTERFACE ADDRESS FLIP FLOP
BOARD ADDRESS REGISTER
CODE CONVERTER
INTERFACE ADDRESS DECODER
BOARD ADDRESS DECODER
LISTEN HANDSHAKE CIRCUITS
BOARD DATA BUS
POWER AND GROUND CONNECTIONS FOR U11, U12 U13, U14, U15, U16, U26, U27, & U28
NOTES.
1. Vcc CONNECTED TO V1 OR V2
2. ALL INVERTERS ARE 74LS04
NATIONAL BUREAU OF STANDARDS
IEEE - 488 INTERFACE BOARD
FOR STEP GENERATION CONTROL UNIT
BOARD 3

Fig. 3.10

	Parameter	Number of Bits	Number of Chips	Circuit Board
(1)	Polarity of transition	1	1	Output
(2)	Level V_1 of step	12	3	DAC/OA
(3)	Level V_2 of step	12	3	DAC/OA
(4)	Pulse repetition period	16	4	Timing
(5)	Pulse length	16	4	Timing
(6)	Pulse length, using delay line	4	1	Timing
(7)	Selection between (5) & (6)	1	1	Timing
(8)	External/Internal clock choice	1	same chip as for (7)	Timing

The values chosen for each of these parameters can be those entered via the user definable keys (see section 6, OPERATING INSTRUCTIONS), or values chosen by a computer program. In either case, the purpose of the interface board is to see to it that the data required to quantify the voltage step parameters are directed to the correct boards, and are accompanied by chip address codes so that each memory chip receives the intended data word.

The chip address decoder located on each board distributes the data words to the correct memory chips on that board, based on the chip address codes received from the interface board.

3.2.3.2 Controller/Interface Operation

A cursory description of the procedure followed by the controller and the interface circuits to perform the required interface functions is given below. Except for DAV signals, the detailed handshake activity will be omitted. A more detailed description of the circuits outlined by dotted lines in figure 3.10 is given in later sections. This procedure is for sending data words to the DAC/OA circuit board from the controller.

	Controller Action	Interface Response
(1)	ATN line set low.[5]	Address decoders U17, U18, and U19 are partly enabled. With DAV signals, (action 2) address decoders U17, U18, and U19 are fully enabled.
(2)	Primary address put on lines DIO1(LSB) - DIO8 (1st data byte). DAV signal sent, i.e., DAV line set low, then high.	This address is compared with primary listen address stored in interface address decoder. If addresses are equal, primary address flag is "set" in interface address flipflop U22.
(3)	Secondary address sent (2nd data byte). DAV signal sent.	This address is compared with secondary listen address stored in interface address decoder. If addresses are equal, secondary address flag is set in U22, and output 2Q high enables U15A and U15B.

[5] Note: 1=low state (<0.8V), 0=high state (>2.0V), per the IEEE-488 standard [10]. "Low" and "high" in this discussion also refer to TTL level negative true logic levels.

(4)	"Selected Device Clear" command sent.	Signal sent via U15A and U26 clears chip address counter U23 to zero. (Code output from U23 is $(0000)_2$).
(5)	ATN line set high.	U15C is enabled via U15B which allows DAV signal to clock the chip address counter U23 (see action 7).
(6)	3rd data byte sent. 1st 3 bits contain board address information. DAV signal sent.	1st 3 bits of data byte are applied to board address register U24. Code applied to register is assumed to be $(000)_2$. Positive DAV pulse is sent via U15C to U16B and U28A. Leading edge of pulse latches board address into U24; trailing edge increases count in U23 by one. Board address decoder then activates line 15 of U06-U09 when strobed by the outputs from U23.
(7)	4th data byte sent (first 4-bit data word for DAC/OA board). DAV signal sent.	4-bit data word from board data bus lines A6, B6, A5, B5 is latched into chip U1 of DAC/OA board (see figure 3.11) by its chip address decoder U7, since code output of U23 of interface board is $(0001)_2$. Data latch signal from U10 is timed with leading edge of DAV pulse. Leading edge of DAV pulse cannot affect U24 as before since $(0001)_2$ code from U23 disables U16B. Therefore, the board address does not change. U16C is enabled, however, allowing DAV to latch board address into U10, thus activating data latch signal to the DAC/OA board. Trailing edge of DAV increases count in U23 to $(0010)_2$.
(8)	5th data byte sent (second 4-bit data word for DAC/OA board).	4-bit data word is latched into chip U2 of DAC/OA board by its chip address decoder U7; latch signal timed with leading edge of next DAV pulse as before.

The above procedure continues until no more data words are to be sent to the DAC/OA board. Then, the unaddressing sequence follows steps (a) through (e) below.

	Controller Action	Interface Response
(a)	ATN line set low.	With step (c), address decoders U17, U18, and U19 are enabled.
(b)	Unlisten command issued, i.e., $(00111111)_2$ sent.	

(c) DAV line set low.	Inputs 1 and 13 of U22 are set low clearing interface address flipflop of address flag information. 2Q output of U22 set low.
(d) DAV line set high.	Inputs 1 and 13 of U22 are reset high.
(e) ATN line set high.	$\overline{\text{NRFD}}$ and $\overline{\text{NDAC}}$ are set low via U14A and U27. (See next section 3.2.3.3 for details).

The overall procedure starting with step (1), and ending with step (e), is now repeated for sending data words to the timing and output circuit boards, with the board address changing to $(001)_2$, and then $(010)_2$ in step 6.

3.2.3.3 Listen Handshake Circuits

These circuits are outlined by dotted lines shown in figure 3.10. The handshake circuits send combinations of $\overline{\text{NRFD}}$ and $\overline{\text{NDAC}}$ to U04, in response to the ATN and DAV signals sent by the controller. The handshake process is fully described in Appendix B of [10].

A handshake sequence is executed by the controller and the interface over the transfer bus each time a byte is transferred over the data bus. Since NRFD and NDAC on the IEEE-488 bus each have two states, the two quantities taken together have a total of four different states (11, 10, 01, 00).

The 1,1 state indicates that the interface is not ready for data (NRFD=1) and has not accepted data (NDAC=1). In this state, communication is temporarily held up on the bus. This state can arise, e.g., if ATN is high and the primary and secondary address flags have not been "set" in the interface address flipflop.

The 0,1 state indicates that the interface is ready for data (NRFD=0) and is not accepting data (NDAC=1). Thus, the interface is prepared to receive messages.

The 1,0 state indicates that the interface is not ready for data (NRFD=1) because it is in the process of accepting data (NDAC=0).

The 0,0 state is an error condition.

Between receiving messages from the controller, the $\overline{\text{NRFD}}$ and $\overline{\text{NDAC}}$ lines of the listen handshake circuits are high so that NRFD and NDAC on the IEEE-488 bus are low and in the 1,1 state. After the controller sets the ATN line low, the normal handshake sequence is as follows: data is put on the data bus when the state is (0,1) indicating that the interface is ready for data. After allowing time for the data to settle, DAV (data valid) is set low by the controller. After DAV is set low, the handshake circuits set NRFD low, followed by NDAC being set high (state 1,0). The latter step tells the controller that the interface has received the data (or address) byte. Following the (1, 0) state, a certain minimum time, T_D, is required for the controller to return DAV to the high state. The circuits in the interface board will function properly with a wide range of T_D values. After DAV is

set high, the NRFD/NDAC state is returned to (0, 1), ready for another handshake cycle. After the message has been received, the controller then sets the ATN line high, and the following inputs are applied to the handshake circuits: (1) the output from U15B is low, (2) the DAV line is high, (3) the ATN and $\overline{\text{ATN}}$ lines are high and low, respectively. Consequently, NRFD and $\overline{\text{NDAC}}$ are set low via U14A, U27, and U14C, U14D.

3.2.3.4 Interface Address Decoder

These circuits are used to decode primary and secondary listen addresses on the data bus, the "Selected Device Clear" command, and the unlisten command. The manner in which the address decoder decodes these addresses and commands will be discussed. Handshake responses will be omitted for the sake of brevity.

Primary Listen and Secondary Addresses

After setting the ATN line low, the controller puts the primary address $(00101000)_2$ on the data bus and sets the DAV line low. To recognize this primary listen address the three inputs to OR gate U12A must all go low, thus providing a rising edge to the 1CK clock input of dual J-K flipflop U22. ATN low and DAV low enable U17, U18, and U19 (3 line to 8 line decoders). Since bit 7 on the data bus is 0, pin 10 of U01 is low, and pin 15 of U17 and pin 13 of U12A are low. Also, since bit 6 is 1, pin 6 of U01 is high and pin 2 of U12A is low. Finally, the first five bits also agree with address 8 set by switch S1. Therefore, output 6 (U21) of comparator pair U20, U21 will be high and pin 1 of U12A low. With all inputs of U12A set low, pin 3 of U22 goes high and $\overline{1Q}$ is set low, as is pin 8 of U13A. Thus, the primary address has been "captured" off the IEEE-488 bus, and the primary address flag "set".

With ATN still low, the controller puts the secondary address $(01101100)_2$ on the bus and sets DAV low. U17, U18, and U19 are again enabled. It can be shown that inputs 9, 10, and 11 of U12B are now low, causing input 9 of U13A to go low. Since pin 8 was previously set low, the positive-going output of U13A is applied to pin 11 of U22, setting 2Q high. Therefore, the secondary address is now captured and the secondary address flag set. It is seen that output 2Q has also set input 9 of U15A and input 1 of U15B high, thus enabling these gates. These conditions are necessary for the operation of the remaining circuits. Also, if U15B were not enabled, the handshake circuits would set the NRFD, NDAC state to (0,0), an error condition as previously mentioned.

Selected Device Clear (SDC) Command

This IEEE-488 bus command clears the chip address counter U23 to zero. The controller keeps ATN low and issues the SDC command, $(00000100)_2$. When DAV is set low by the controller, U17, U18, and U19 are enabled, and the outputs from U01 and U02 cause all inputs of U11B to go low. Output 12 of U11B goes high, and since U15A was previously enabled, a clear signal is applied to U23, setting outputs QA, QB, QC, and QD of the counter to low (output code of $(0000)_2$). These lows are applied to pins 2, 3, 11, and 12 of U13C and U13D, producing a high at pin 6 of U16A and pin 2 of U16B, enabling the latter. Note that after the first count has been given to U23, U16B is then disabled and U16C is enabled. (See steps 6, 7, and 8 of section 3.2.3.2).

Unlisten Command

When no more data bytes are to be sent, which is determined by the controller, the ATN line is set low and the unaddressing sequence begins. (See step (a)-(e) of section 3.2.3.2). With ATN set low, the controller issues the unlisten command $(00111111)_2$. The controller also sets DAV low, enabling U17, U18, and U19. The above code sets lines 3, 6, 10, and 14 of U02 and lines 3 and 6 of U01 high. Line 10 of U01 is set low. It can be seen that these inputs to U17, U18, and U19 cause lows on the inputs of U12C and, therefore, a low at input 1 (1 CLR) and input 13 (2 CLR) of U22. This signal clears flipflop U22 of address flags. When DAV goes high, inputs 1 and 13 of U22 are set high. The controller may then proceed to issue an untalk command $(10111111)_2$, to which only the handshake circuits respond. The controller sets ATN high, ending the command sequence.

3.2.3.5 Code Converter

IC U05 is a 4-bit binary full adder which is used to translate ASCII characters to hexidecimal digits. Lines 3, 6, 10, and 14 of U02 and line 3 of U01 are connected to the adder, as shown in Fig. 3.10. If the incoming data is an ASCII "0" to "9", the adder takes no action. If the incoming data is an ASCII "A" to "F" (the signal applied to B1 and B4 is high), a 9 is added to the first 4 bits to obtain a sequence of numbers in the range of 0 to 15. This allows entry of the hex digits, A to F, from the controller keyboard or in a program mode. The data output lines of U05 are connected by backplane wiring to the three control unit circuit boards mentioned previously. The inactive boards cannot access this data, however, because the chip address lines are held high and the chip address decoder receives no latch signals.

3.2.3.6 Board Address Decoder

This circuit employs ICs U06-U10. The three lines of the board address register U24 are connected to the inputs of U06 through U10, which are three line to eight line decoders. For example, if the register output is $(000)_2$, output Y_0 (pin 15) of the five chips is active. If the register output is $(001)_2$, output Y (pin 14) of the five chips, is active, etc. Outputs Y_3 through Y_7 are not used. Outputs Y_0 are connected to the DAC/OA board, outputs Y_1 to the timing board, and outputs Y_2 to the output board. Outputs which are inactive at any time are held high.

Outputs QA, QB, QC, and QD of chip address counter U23 are applied to pin 4 (G2A) of U06, U07, U08, and U09, respectively, and are used to latch the active output lines of U06-U09. These lines are connected to the chip address decoder located on the activated board. The decoder determines which chip is to receive the data sent to the board. Each chip address is latched into the decoder by a data latch signal received from the active output line of U10. The latch signal occurs when DAV is passed through U16C and U28C to pin 4 (G2A) of U10.

Succeeding data bytes are handled by the interface in the same way, with the chip address counter advancing one count with each DAV pulse. Thus, the counter and ICs U06-U09 serve as a chip address encoder. When all chips have received data for the selected board, the chip address counter is reset to zero as before by the SDC command, and the process just outlined is repeated for the next board, etc.

3.2.4 DAC/OA Board

The DAC/OA board contains the circuits necessary to generate voltage V_A and V_B (see figure 3.11). If V_1 and V_2 are the initial and final voltage levels of the desired voltage step, respectively, then

$$V_A = 2 * V_2,$$

and

$$V_B = \text{sign}\,(V_2 - V_1) * (\,|V_2 - V_1| + 8.3),$$

where * indicates multiplication, the sign function is -1 if $V_2 > V_1$, and is +1 if $V_2 < V_1$. In order to have approximately 10% overrange capability for V_2 and V_1, the ranges for V_A and V_B are set at ± 11 V and ± 20 V, respectively.

Voltages V_A and V_B are generated by a pair of D/A converters (DACs) with output amplifiers (OAs). Since the DACs for both supplies have an output range of $\pm$ 10 V, the nominal amplifier gains for the V_A and V_B supplies are set at 1.1 and 2.0 respectively. Therefore, these ratios are used for R2/R1 and R4/R3, respectively, in amplifiers U_A and U_B.

If V'_A and V'_B are the output voltages from DAC A and DAC B, respectively, then

$$V'_A = -\,0.909091 * V_A\,,$$

and

$$V'_B = -\,(1/2) * V_B\,.$$

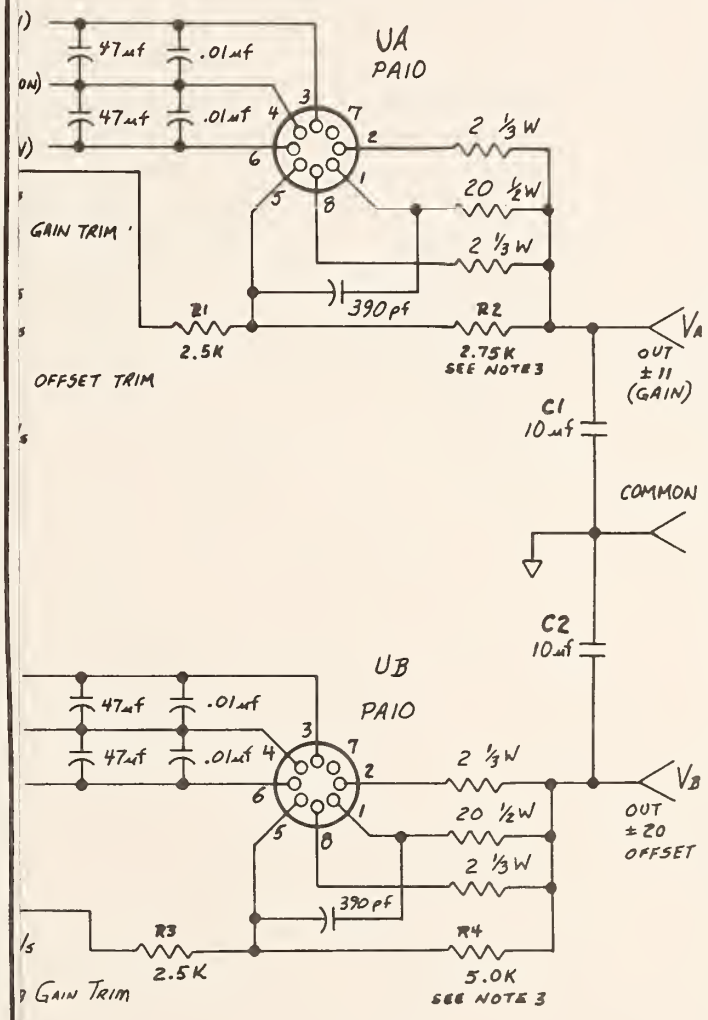
The networks in the output circuits of amplifiers UA and UB, including C1 and C2, are recommended by the manufacturer to improve the load transient response.

Complementary offset binary coding is used for both DACs. Registers U1, U2, and U3 provide the input code for DAC A and registers U4, U5, and U6 provide the input code for DAC B.

The inputs to the chip address decoder (U7) are obtained from outputs Y_0 of U06-U09 of the board address decoder shown in figure 3.10. As the input code changes one bit at a time from $(0001)_2$ to $(0110)_2$, 4-bit data words from the board data bus are sequentially loaded into registers U1 through U6. The data latch signal on line C8 and on G1 and G2 of U7 is the gated DAV pulse from the IEEE-488 interface board. Since the selected output line of U7 goes low when G1 and G2 go low, the flipflops in the selected register are triggered on the leading (negative going) edge of DAV. The complete process by which the address code and the data words are obtained (for registers U1-U6) is explained in section 3.2.3.

The board address $(0000)_2$ and the six 4-bit data words, needed to establish V'_A and V'_B, are contained in a 7-digit hexadecimal word string, which may be entered via the keyboard or a computer program. The make-up of the DAC/OA board word string is discussed further in section 4., DRIVER SOFTWARE.

ORIGINAL DATE OF DRAWING 29 MAR 85			
REVISIONS			
NO	E C N	CHANGE	DATE
1	1	UPDATE	3/19/86
2		ADDED U10	5/27/86
3			
4			



⅛ Offset Trim

IN OHMS
PIN-OUTS = □

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

DAC/OA BOARD

FOR STEP GEN. CONTROL UNIT

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN PALM	CHECKED
TOLERANCES (Unless otherwise specified)	PROJECT ENGR DF	PROJECT ENGR
DECIMALS ± .005 FRACTIONS ± .015 ANGLES ± ½°	SUBMITTED BY CHIEF SEC.	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC. 722	THIS PRINT ISSUED	APPROVED BY CHIEF DIV.

g. 3.11

ARD 7

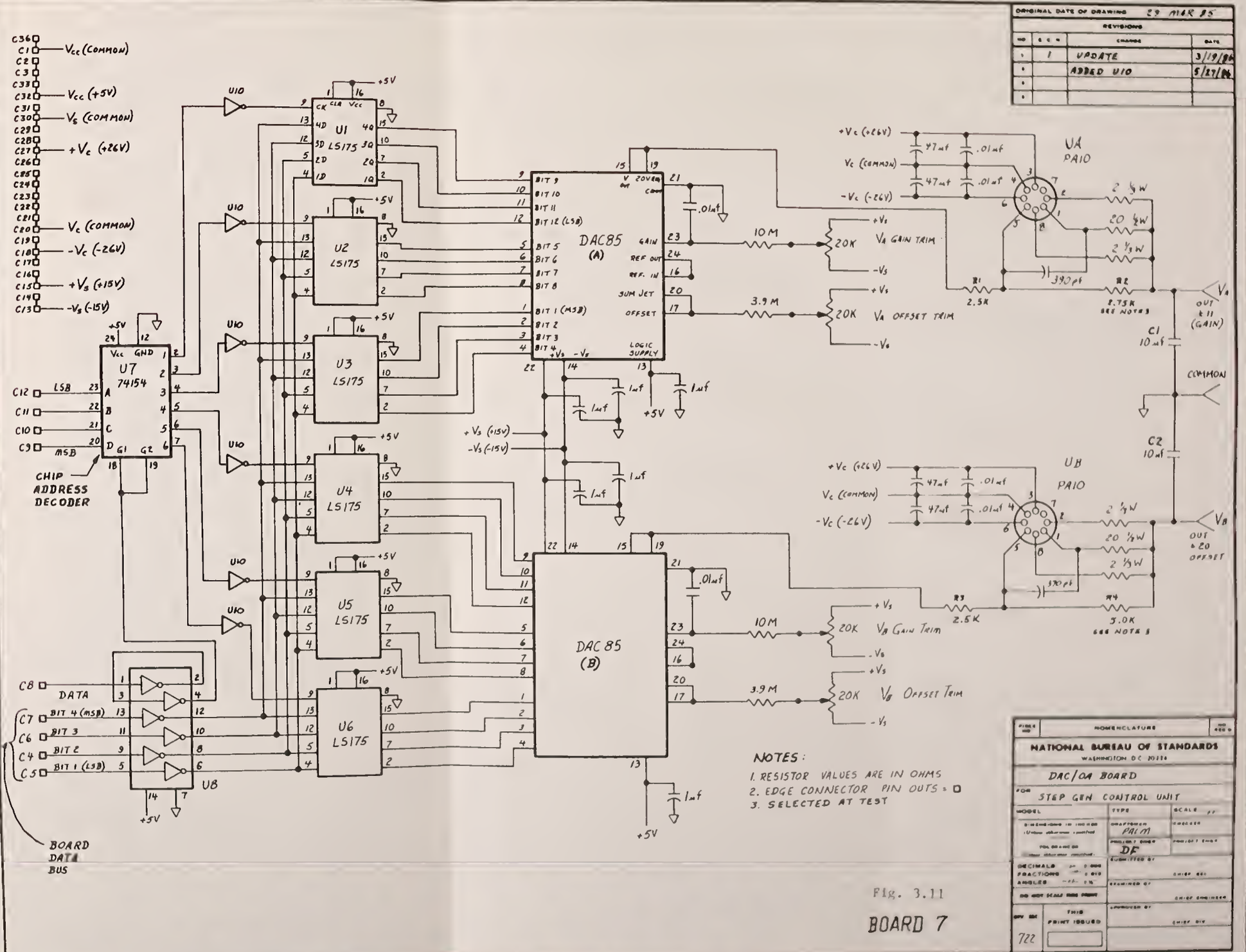


Fig. 3.11

BOARD 7

3.2.5 Timing Board

The circuits on the timing board (see figure 3.12) control the pulse repetition period and the pulse length of the voltage steps as well as the internal/external clock choice. The inputs to the chip address decoder U11 are obtained from outputs Y1 of U06-U09 of the board address decoder shown in figure 3.10. As the input code changes one bit at a time from $(1001)_2$ to $(1010)_2$, 4-bit data words from the board data bus are sequentially loaded into registers U1 through U10. The latching signal on line C14 and G1 and G2 is the gated DAV pulse from the IEEE-488 interface board, and appears on the selected output line of U11. The data word is latched into the selected register by the leading edge of this pulse after it is inverted by one of the U18 or U19 inverters.

The data words (codes) that have been latched into registers U3-U10 are preset into counters U21-U28 once each output pulse repetition period. Timing of the presetting occurs with the first negative transition of the clock signal after the load input (pin 9) of the counters is set low.

The pulse repetition period of the step generator is determined by the code value preset into counters U21 through U24, and equals the complement of this code times the (10 MHz) clock period. When these counters receive a full count, the code values in registers U3-U6 are preset into these counters. The code values in registers U7-U10 are also preset into counters U25 through U28 at the same time. These latter ICs are used to control the pulse length, which is discussed next.

Outputs 3 and 6 of U1 are applied to U12 to select either the internal clock (U16) pulses or the external clock pulses from line A17. Outputs 11 and 14 of U1 are applied to U13 to select the means of controlling the pulse length. The function table for U13 is shown below:

	B	A	$1C_0$	$1C_1$	$1C_2$	$1C_3$	1Y
1.	L	H	x	L	x	x	L
2.	H	L	x	x	H	x	H
3.	L	L	L	x	x	x	L
4.	L	L	H	x	x	x	H
5.	H	H	x	x	x	L	L
6.	H	H	x	x	x	H	H

Thus, when inputs A and B are both low the output waveform (at 1Y) is determined by the input pulse to $1C_0$. The length of this pulse is determined by the binary code preset into counters U25 through U28, and is equal to the complement of this code times the (10 MHz) clock period. Pulse lengths ranging from 100 ns to ~6 ms may be selected (see section 4.1.1.2).

This same pulse is applied to U20 and delay line U15, and appears at the output of U29 and input $1C_3$ of U13. However, this pulse is terminated by the delayed pulse through U15. Therefore, the length of the pulse at $1C_3$ equals the delay of U15, which is programmed via U2. This method provides for pulse lengths in the range of 15 to 165 ns (see section 4.1.1.2). The pulse at $1C_3$ appears at output 1Y of U13 when inputs A and B are both high. Output pin 1Y

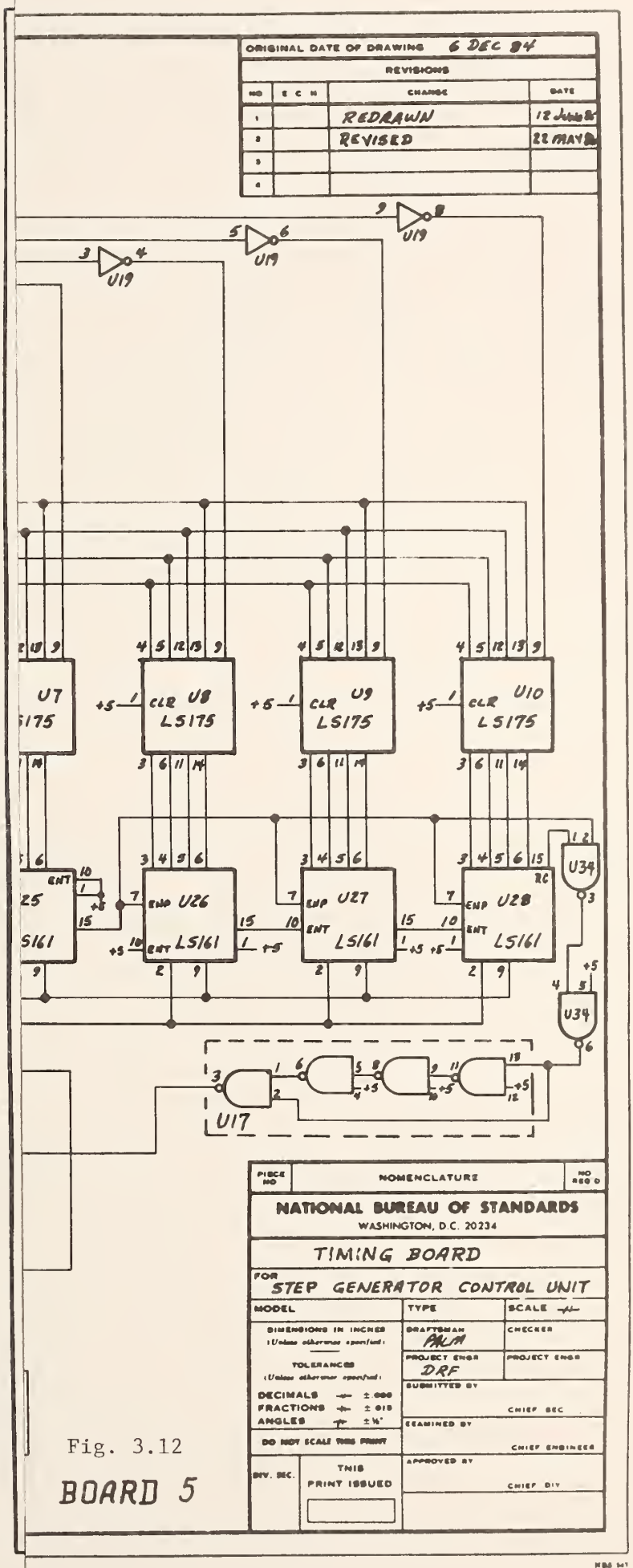


Fig. 3.12

BOARD 5

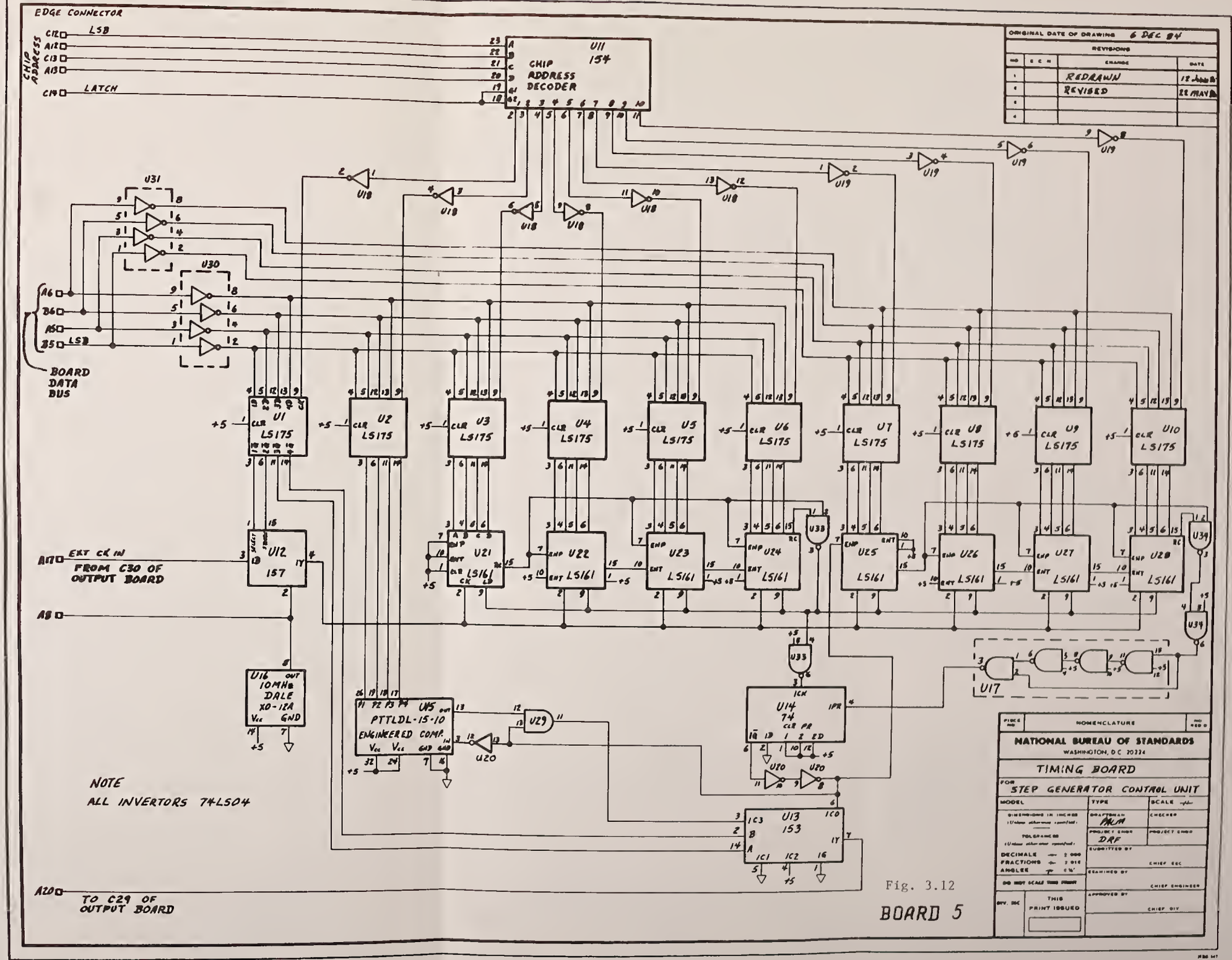


Fig. 3.12

BOARD 5

is connected via A20 and C29 to pin 2 of U3 on the Output Board (see figure 3.13). The function table also shows that steady-state values are produced at 1Y for HL and LH combinations of A and B, respectively. Therefore, dc levels of either V1 or V_2, as well as transitions between these levels, can be selected for the step generator output by programming the states of the A and B inputs to U13.

The complete process by which the chip address code and the data words are obtained (for the registers U1-U10) is explained in section 3.2.3.

The board address $(001)_2$, pulse length and repetition period, internal/external clock choice, and other quantities are selected by an 11 digit hexadecimal word string, which may be entered via the keyboard or a computer program. The composition of the timing board word string is described in section 4., DRIVER SOFTWARE.

3.2.6 Output Board

The circuits for selecting the polarity of voltage steps, under program control, are located on the output board and shown in figure 3.13. Also shown are circuits for receiving an external TTL compatible clock signal, and for outputting TTL timing signals.

External clock pulses, input at J4, are applied to U4 using a coaxial cable, and the output of U4 is applied to C30 and routed to A17 of the timing board. The TTL timing signal received from the timing board is wired to have both an undelayed output and an output with 150 ns delay, obtained by using delay line U5. These outputs are available at J6 and J5, respectively.

A TTL level pulse of at least 1.5 ms duration is required from Q1 to set the relays in the step generator output circuit for negative steps. A similar pulse is required at the output of Q2 to set the relays for positive steps. The corresponding logic states for the signal lines leading to Q1 and Q2 are as follows:

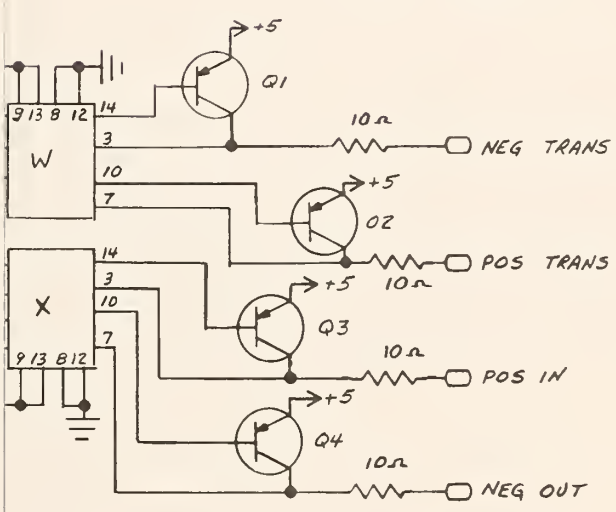
	U6 Input (pin no.)				U2				Transistors	
	9	5	3	1	4Q	3Q	2Q	1Q	Q2	Q1
(1)	x	x	L	H	x	x	H	L	L	H
(2)	x	x	H	L	x	x	L	H	H	L
(3)	x	x	L	L	x	x	H	H	L	L

States (1) and (2) must be latched into U2 and held for at least 1.5 ms to operate the relays. The logic levels for the U6 inputs may be changed after the signals are latched into U2. Thus, three different input words are required from the board data bus: $(xx01)_2$, $(xx10)_2$, and $(xx00)_2$.

Operation of these relay driver circuits can be described with an example. Assume that state (3) exists initially and that a negative transition is desired. The procedural steps described in 3.2.3.2 are followed, except that the board address is $(010)_2$ and the board address decoder activates lines 13 (Y_2) of U06-U10 on the IEEE-488 interface board. Also, from the fourth data byte (step 7), the 4-bit data word sent to the input of U6 is $(xx01)_2$. The second DAV signal, applied to U6 via U1, latches the data word into U2 and the Q1 output goes high. The controller now issues

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1	REV A	CHANGED PIN NOS	2-20-75
2			
3			
4			

Q1 - Q4 = 2N2905



PIECE NO	NOMENCLATURE	NO REQ'D
NATIONAL BUREAU OF STANDARDS WASHINGTON, D.C. 20234		
OUTPUT BOARD		
FOR STEP GENERATOR CONTROL UNIT		
MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKED
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ± .000 FRACTIONS ± 1/16 ANGLES ± ½°	SUBMITTED BY CHIEF EEC	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
GOV. SEC.	THIS PRINT ISSUED	APPROVED BY CHIEF DIV

ig. 3.13

OARD 9

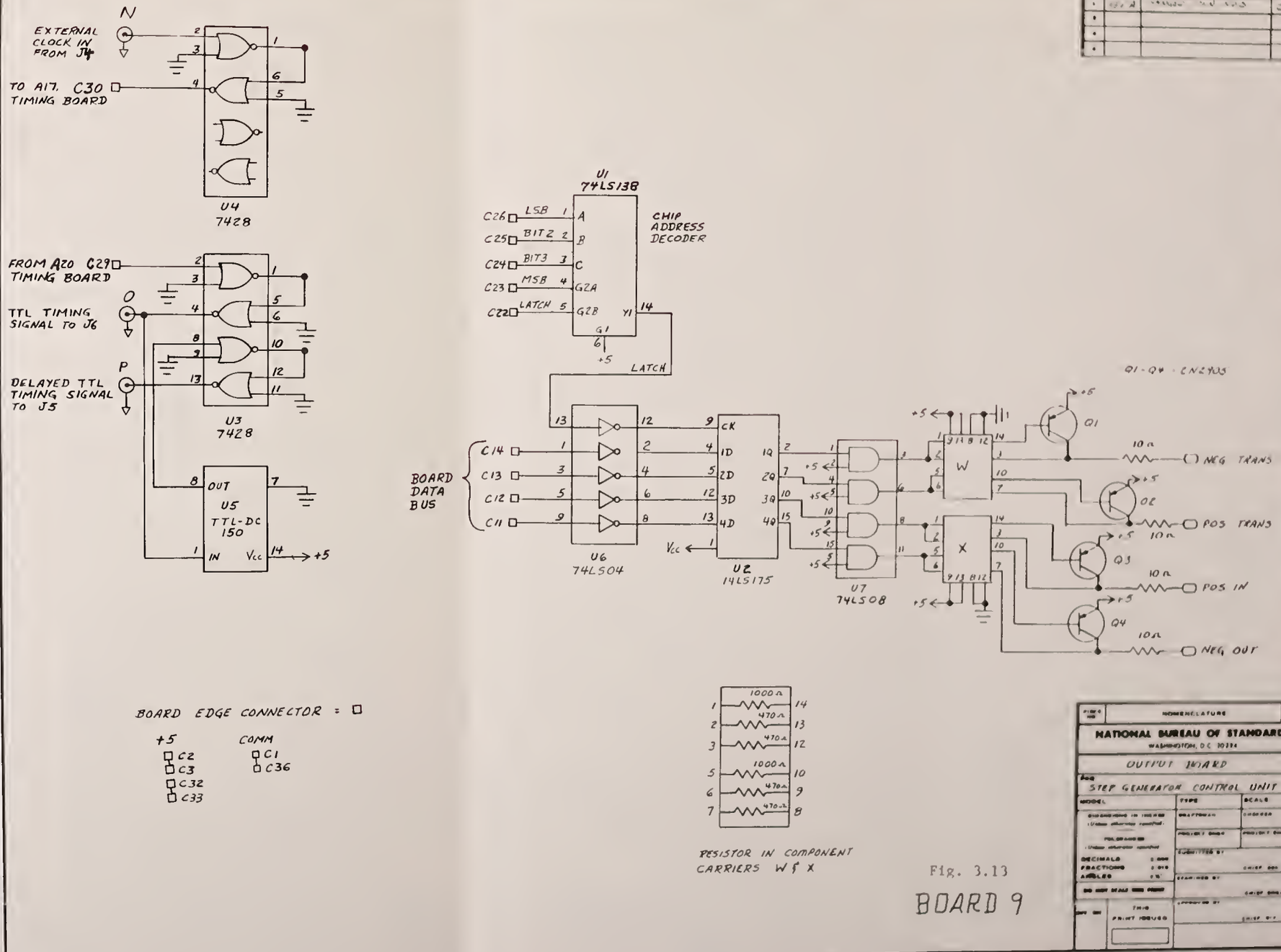


Fig. 3.13

BOARD 9

the unaddressing sequence (steps (a)-(e)) of section 3.2.3.2. When the sequence is complete, the controller repeats the above procedure, except that this time the data word applied to U6 is $(xx00)_2$. This sets the output of Q1 to the low state. The time consumed between corresponding points in the two commands is approximately 5 ms, and determines the relay latching pulse length. The procedure is the same for a positive transition, except that the first data word applied to U6 is $(0010)_2$ for activating Q2. Transistors Q3 and Q4 are not used in this application.

3.2.7 Fixed Power Supplies

Several fixed, regulated power supply voltages are required for powering the circuits boards described in the previous sections (see figure 3.9). The + 5 V and - 5 V power supplies (1.5 A each), required for the step generator test head, are mounted on board 15. The $\pm$ 15 V supply (one module), required for the test head, is mounted on board 11. Also mounted on the latter board is the $\pm$ 15 V supply (one module), required for operating the DACs on board 7. All 15 V supplies have a 200 mA capacity. The + 26 V and - 26 V supplies (300 mA each), mounted on board 19, are required to operate the output amplifiers (U_A, U_B) on board 7. In addition to the board-mounted supplies, a 3 A, 5 V logic supply is mounted on the rear panel of the control unit.

4. DRIVER SOFTWARE

4.1 VSG Driver Program[6]

The VSG driver program is listed in Appendix B. The numeric and string variables and the line labels used in this program are all defined there. Also given are flow charts for each of the user definable keys and for GOSUB 2500, the main routine used to calculate codes needed for the DACs (see figure 3.11).

The VSG driver program facilitates operating the step generator system by the user-definable keys of the computer (controller/processor). (see section 6. OPERATING INSTRUCTIONS). The program generates the necessary board string variables from the pulse parameter values entered on the keyboard. Each string variable identifies the circuit board that controls the parameter (or parameters) being quantified by the keyboard entries, and the data words to be sent to specific registers on the board. In addition to computing data words from the parameter values, the program also flags unacceptable (illegal) parameter values, such as $V_1 = V_2$ or pulse length > pulse period.

4.1.1 Coding to the Storage Registers

The IEEE-488 bus interface board has an adder circuit in the data lines to the registers in the control unit. Allowable ASCII symbols that can be set are 0-9, A, B, C, D, E and F. When letters A-F are sent, bit 5 of the ASCII character enables the adder and adds 9 to bits 1 to 4 (bit 1 = LSB) to obtain a hexidecimal code. This allows use of characters A-F from the keyboard or in a programmable mode. In the explanations of the string variable for each board, the use of 0-9 and A-F refer to ASCII inputs from the computer to the IEEE-488 interface.

Note: to ensure reliable loading of data into storage registers, the internal/external clock is turned <u>off</u> while loading data (see the timing board functions in section 4.1.1.2).

4.1.1.1 DAC/OA Board String Variable DAC $

Position	1	2	3	4	5	6	7	Each position
Code	0	LSHD	+1	MSHD	LSHD	+1	MSHD	4 bits wide

Bit location in each position:

Position Number			
LSB	+1	+2	MSB

[6] The notation, voltage step generator (VSG), is used interchangeably with numeric variable Vsg (in Appendix B), and step generator (SG).

LSHD = least significant hex digit; + 1 = second hex digit
MSHD = most significant hex digit
LSB = least significant bit; + 1 = second bit; + 2 = third bit
MSB = most significant bit

Position 1: Board address. Set to "0" for DAC/OA board address.

Positions 2-4: Hex code for DAC A. Coding is complementary offset binary and output voltage range of DAC A is +/- 10 volts.

Positions 5-7: Hex code for DAC B. Coding is complementary offset binary and output voltage of DAC B is +/- 10 volts.

Note: See restrictions in section 3.2.4 regarding allowable voltages when positive or negative transitions are used.

4.1.1.2 Timing Board String Variable Time $

1	2	3	4	5	6	7	8	9	10	11
1	Func	Delay	LSHD	+1	+2	MSHD	LSHD	+1	+2	MSHD

POSITION	FUNCTION
1	Board address
2	Selects timing board functions
3	Program pulse length using delay line
4-7	Sets the voltage-step generator drive frequency
8-11	Sets the pulse length

Position 1: Set to "1", the timing board address
Position 2: Selects timing board functions

Code

"0" Numeric variables C1=0, C2=0; internal clock, VSG drive frequency, and pulse length set by programmable counters.

"1" Numeric variables C1=1, C2=0; external clock, VSG drive frequency, and pulse length set by programmable counters.

"2" Numeric variables C1=2, C2=0; turn internal/external clock off.

"5" Numeric variables C1=1, C2=4; initial level output, the internal/external clock is turned off.

"9" Numeric variables C1=1, C2=8; final level output, the internal/external clock is turned off.

"C" Numeric variables C1=0, C2=12; pulse length set with delay line using internal clock. This must be set before using Key 5.

"D" Numeric variables C1=1, C2=12; pulse length set with delay line using external clock. This must be set before using Key 5.

Position 3: Program pulse length using delay line. This is used after "C" or "D" set in position 2. The coding is in one hex digit, "0" = smallest step size of 15 ns (the initial delay), then in 10 ns steps to 165 ns for "F". Minimum step size that propagates thru the system is about 35 ns, a "2". Note: pulse length must be set to a value greater than one multiplied by (internal or external clock periods).

Positions 4-7: Divide the internal/external clock frequency by an integer from 2 to 65,535 to obtain the VSG drive frequency. Coding for each digit is in hexadecimal.

Positions 8-11: Set the pulse length in clock periods (internal or external) multiplied by an integer from 1 to 65,534. Coding for each digit is in hexadecimal. Note: when setting up the VSG drive frequency, the pulse length must be less than the period of the VSG drive frequency.

4.1.1.3 Output Board String Variable "XX"

Position:	1	2	Each position
Code	2	C	4 bits wide

Position 1: Board address. Set to a "2" for output board address.

Position 2: Transition code (polarity of step change).

Code

"0" Normal and initialization setting.

"2" Positive transition; should be set to "2" for about 5 ms, then set back to "0".

"1" Negative transition; should be set to "1" for about 5 ms, then set back to "0".

4.2 Computer/IEEE-488 Interface Code

Decimal 7 is a selection code used by the HP9000 series 200 computer to address the accessory slot in the computer where the IEEE-488(GP1B) interface is installed. This interface select code is not sent out on the IEEE-488 bus. The following two examples illustrate the use of this code.

Example 1: Selected Device Clear

CLEAR 70812 = Selected device clear,

where 08 is the primary listen address set by S1 on the interface board (figure 3.10) and 12 is the secondary address. After the primary and secondary address are set in the address register, the selected device clear command is executed.

Example 2: Output data

```
OUTPUT 70812; AXX ... XX,
```

where

A = board address (0, 1 or 2)

XX ... XX = ASCII data to storage registers.

The storage register for the board address is IC U24 on the IEEE-488 interface board.

5. SPECIFICATIONS

The performance specifications of the NBS Step Generator system are given below in Table 1. Static, step, and exponential waveform errors are given in terms of either the 10 V full scale range (FSR) or the 2 V FSR. The polarity selected by the operator corresponds to the transition between V_1 and V_2, the initial and final values of a step, respectively. Settling times to within ± 0.1% of FSR and within ± 0.02% of FSR are listed under "Step Limitations". Self-heating effects on the V_2 level are listed under "Duty Cycle Dependence".

Table 1
Typical Performance Specfications

Static Errors	Level V_2	Level V_1	
Offset (software corrected)	0.01	1.0	% FSR
Gain (software corrected)	0.01	1.0	% FSR
Linearity (Max.)	0.008	0.5	
Quantization uncertainity	0.012	0.024	% FSR
Noise (40 MHz BW)	<500	<500	µV p-p
Step Limitations	**± 5 V Range**	**± 1 V Range**	
Transition Duration	7	6	ns
Settling Time			
0.1%	19	15	ns
0.02%	26	22	ns
Equivalent Bandwidth	50	58	MHz
Droop/Flatness/Aberrations After Settling	<0.02	<0.02	% FSR
Exponential Waveform Errors	**0.55 µs**	**27.5 µs**	
Deviation From Ideal Waveform			
Max.	0.05*	0.02**	% FSR
rms	0.01*	0.01**	% FSR

*Not including 1st 10% of waveform. **Not including 1st 5% of waveform.

Duty Cycle Dependence		
V_2 Level Change With Duty Cycle (5-95%)		
0=100 ms	<0.02	% FSR
Max. Final Change (30 s)	<0.05	% FSR

Ranges of Other Pulse Parameters:

- Pulse Repetition Rate - 153 Hz to 3.3 MHz; to 5 MHz with external clock
- Pulse Length - 20 ns to ~ 6 ms
- Duty Cycle - approximately 5% to 95%

6. OPERATING INSTRUCTIONS

Drawings of the front and rear panels of the NBS Step Generator control unit are shown in Figs. 6.1 and 6.2. The control unit should first be checked out for correct operation before connecting the umbilical cable of the test head to the front panel. The functions and voltages for connector J7 pins are listed in Table 2. The signals on pins 1-5 are generated under computer control. After correct operation of the control unit has been verified, connect the test head umbilical to connector J7. Connector J2 ($\pm$ 1 V range) of the test head must be terminated in a 50 Ω impedance, either a coaxial termination or the input impedance of the instrument under test. Connector J3 which accepts the timing signal, may be connected to either J5 or J6.

The primary address of the control unit has been set to 8. If the address must be changed, the address switch is located on the IEEE-488 Interface Board (#3). To gain access, the front panel must first be removed, and the board pulled from the chasis (see installation instructions sent with instrument). Addresses 1-31 may be set with the address switch. The switch is coded in binary negative true logic, where the MSB is position 1 and the LSB is position 5. The secondary address of the control unit is 12, and is hard-wired into the interface board.

The software for operating the control unit was written in BASIC 3.0 language for use with HP 9000 series 200 computers. The accompanying driver software permits simple selection and entry of all programmable functions. The basic features with user definable key numbers include:

Key 0 Initiation routine. The step generator must be initialized before using the remainder of the driver software. The initialization parameters (for the 10 MHz internal clock) are:

- repetition rate is 50 kHz
- pulse length is 5.0 μs (50 clock periods)
- transition is positive
- initial level is - 1 V
- final level is + 1 V
- internal clock is selected
- programmable frequency and pulse length mode selected
- clock is enabled

Key 1 Reserved for future use.

Key 2 Sets the polarity of the transition, and the final and initial voltage levels for the $\pm$ 5 V range.

Key 3 Sets the repetition rate of the output step pulse train with a range of 153 Hz to 5.0 MHz using the internal clock. The software calculates the closest allowed frequency to the one selected, based on the requirement that the clock frequency be an integral multiple of the selected frequency.

Key 4 Sets the pulse length (duration of the final level) in increments of 100 ns when using the internal clock, otherwise in increments of the external clock period.

Key 5 Sets the pulse length using a programmable delay line to obtain pulses shorter than those obtainable with key 4. This function will have been previously set with keys 7 or 8. The pulse length is set in 10 ns increments from 20 ns to 160 ns. When using this key, the pulse length set by key 4 must be set to 200 ns or greater.

Key 6 Sets the pulse length and frequency by an integer procedure. The pulse length is set by entering the desired number of clock periods of the internal or external clock. The period of repetition is simliarly set by entering an integer multiplier (2-65,535) of the clock period. Pulse lengths greater than the period of repetition should not be entered.

Key 7 Displays on the screen the timing board functions and codes needed to obtain these functions. Variables C_1 and C_2 are entered to obtain the functions.

Key 8 Permits entering C_1 and C_2 without displaying the timing board functions.

Key 9 Reserved for future use.

Key 10 Status. Gives the repetition rate, pulse length, transition polarity, voltage levels, and clock selected (internal or external).

Key 11 Change the transition. The initial and final voltage levels are interchanged.

Key 12 Enables/disables clock.

Key 13 Change the final voltage level.

Key 14 Change the initial voltage level.

Keys 15-20 Reserved for future use.

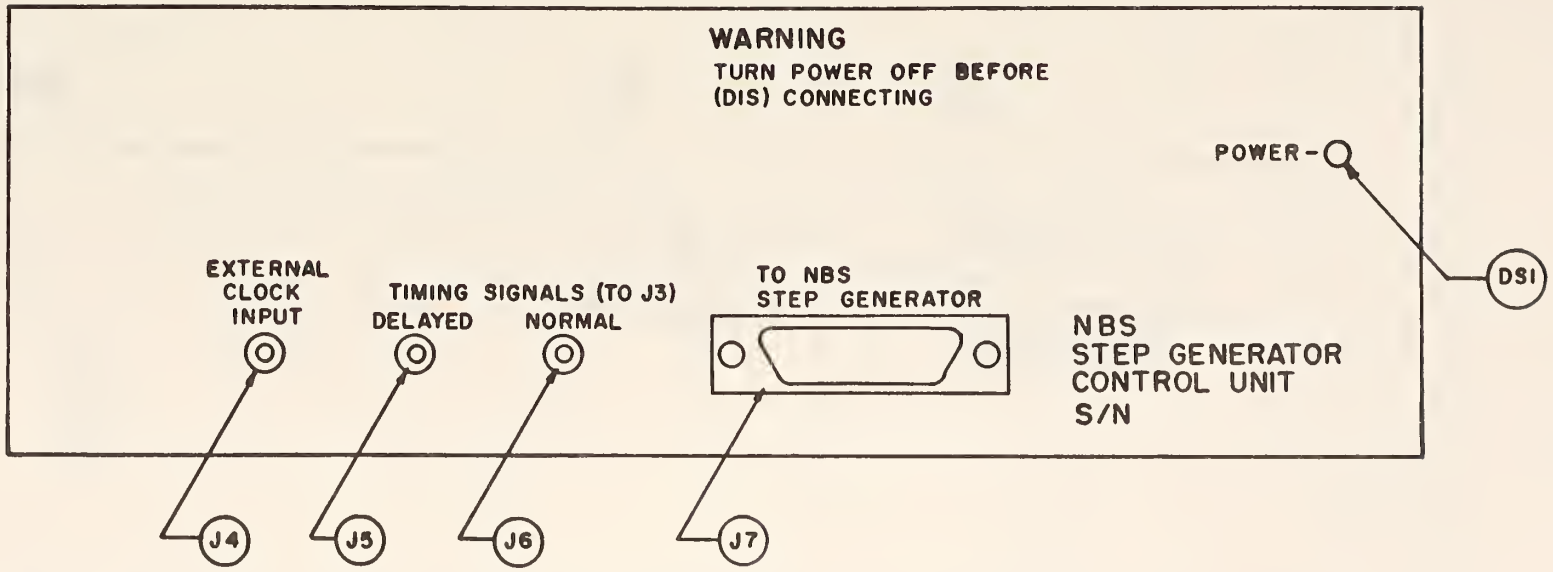


Fig. 6.1 Front panel connectors. Connector J4 permits external synchronization of the TTL timing signals output by J5 and J6. The signal from J5 is delayed 150 ns relative to that from J6. The umbilical cable to the step generator output circuit is connected to J7. DSI is an LED for power ON/OFF indication.

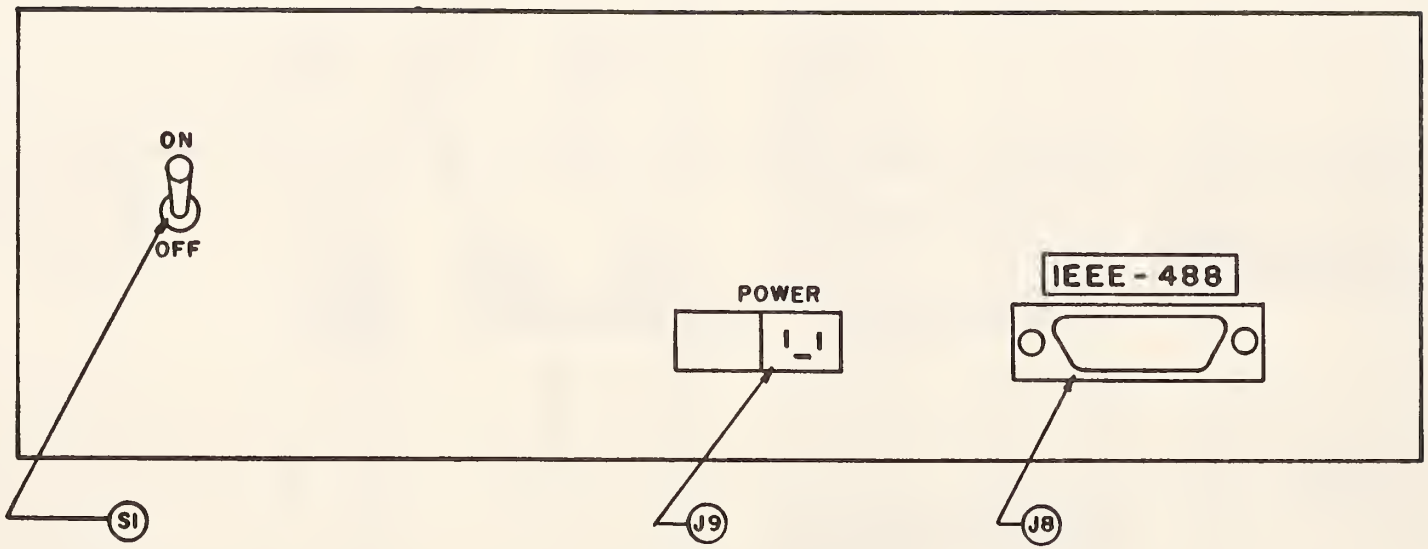


Fig. 6.2 Rear panel connectors and power switch (S1). J9 is the power line connector (120 V) with an integral 3A fuse. The IEEE-488 bus to the controller is connected to J8.

Table 2

Functions and Voltages for Connector J7 Pins
Values Given for V_A and V_B are Outside Limits
(See Note at Bottom of Table)

Pin No.	Function/Voltage
1 & 2	$V_A/\pm$ 11 V
3	$V_B/\pm$ 20 V
4	Neg. Pol. Relay Drive/TTl. Pulses approx. 5 ms wide
5	Pos. Pol. Relay Drive/TTL. Pulses approx. 5 ms wide.
6 & 7	N. C.
8 & 9	Supply/ + 5 V $\pm$ 0.2 V
10	Supply/ - 5 V $\pm$ 0.2 V
11 & 12	N. C.
13 & 14	V_A Return/0 V
15	V_B Return/0 V
16	Relay Returns/0 V
17	Supply/ + 15 V $\pm$ 0.3 V
18	Supply/ - 15 V $\pm$ 0.3 V
19	$\pm$ 15 V Return/0 V
20 & 21	+ 5 V Return/0 V
22	- 5 V Return/0 V
23 & 24	N. C.

Note: Under program control, $V_A = 2 * V_2$ and
$V_B = \text{sign}\ (V_2-V_1)*(|V_2-V_1|+8.3)$, where
* indicates multiplication, the sign function is
-1 if $V_2 > V_1$, and is + 1 if
$V_2 < V_1$. $V_2 = V_1$ is a disallowed condition.

7. TESTING

7.1 Static Testing

The static errors of the NBS Step Generator system have been measured over the full range at the step generator's output terminals using a precision DVM. Offset and gain errors are corrected in the system software using data from periodic calibration. The measured maximum independently based linearity error at the V_2 level is 0.008 percent of full-scale range. Figure 7.1 is a typical linearity error plot of V_2.

The noise at the generator's output has also been measured at the $\pm$ 5 V output terminal, with the peak-to-peak value found to be less than 500 μV in a 40 MHz bandwidth.

A complete list of the static errors for both of the V_2 and V_1 levels of voltage steps is given in Table 1 of section 5. SPECIFICATIONS. Also shown in that table is the quantization uncertainty. This uncertainty is caused by the lack of resolution in the programmable power supplies (V_A, V_B), from which V_2 and V_1 are derived.

If the device under test (DUT) has a 50 Ω input impedance, connector J2 ($\pm$ 1 V range) should be connected to the DUT input without using a coaxial termination (see section 3.1). Voltage uncertainty, caused by DUT input impedance uncertainty, can be removed by static measurements of V_2 and V_1. Static measurements can be made at the DUT input with a DVM by placing a BNC T-connector between J2 and the DUT input.

7.2 Measurement of Voltage Step Characteristics

A sampling voltage tracker (SVT), peak detector circuits, and a sampling oscilloscope were used to characterize the output waveforms of the step generator. The SVT and peak detector were used for settling time (ST) measurements, and the SVT and sampling oscilloscope were used for transition duration measurements. The sampling voltage tracker has been used previously for similar measurements [2], [8], [11], [12], and [13].

The basic SVT consists of a high-speed sampling comparator and a voltage integrator in a feedback loop, and can be represented by figure 7.2. The strobe pulses, 5 to 10 ns wide, cause the input waveform f(t) to be sampled (compared with the output voltage V_D of the integrator) at instants in time coinciding with the trailing edges of these pulses. Assume that the period of f(t) is T and that the value $f(t_1)$ is to be measured. Then, the strobe pulses must be timed to sample f(t) at times t_1, $t_1 + T$, $t_1 + 2T\cdots$. The result of these comparisons is to drive V_D positive or negative until it nearly equals the value of f(t) at the instants of comparison. If some other value of f(t), say $f(t_2)$, is to be measured, f(t) must be sampled at times t_2, $t_2 + T$, $t_2 + 2T,\cdots$, etc.

The SVT was employed in the automatic measuring system shown in figure 7.3 with the delay generator programmed to have delay steps (increments) of 0.5 ns. The maximum allowable voltage range for the comparator in the SVT is

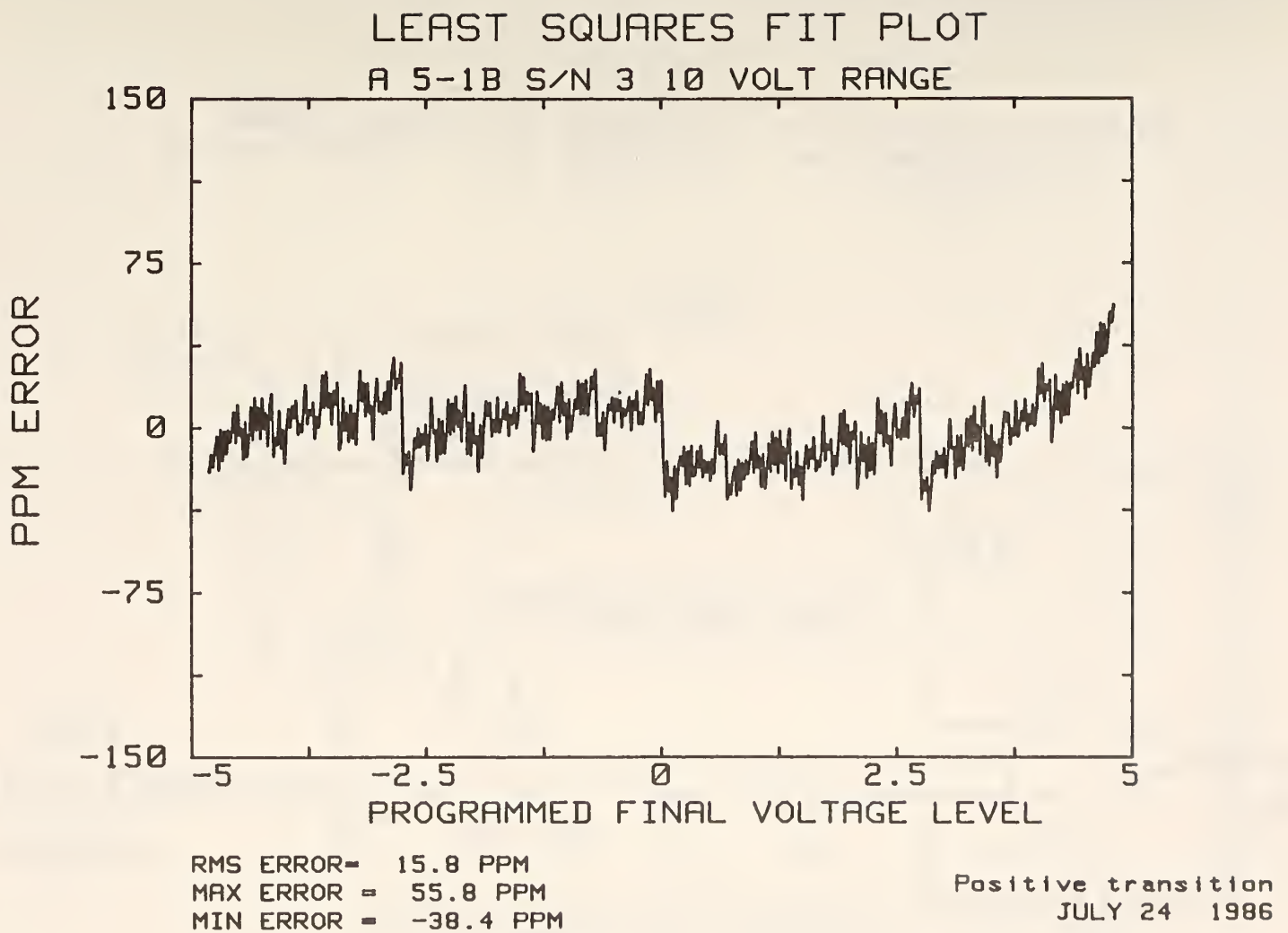


Fig. 7.1 Least squares fit in ppm of linearity error of V_2 from +5 V to -5 V, with quantization error removed.

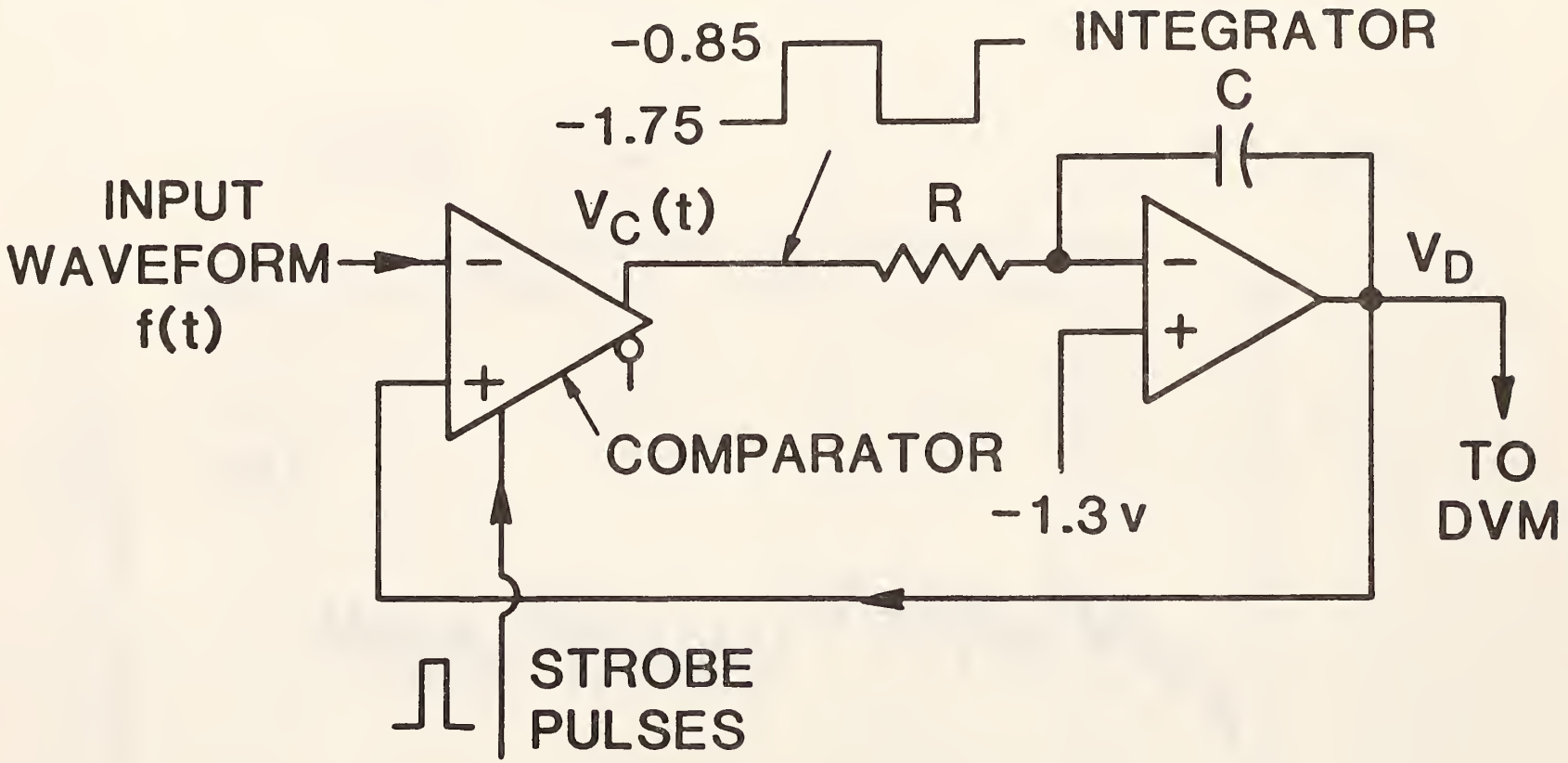


Fig. 7.2 Basic sampling voltage tracker (SVT). Input waveform f(t) is sampled (compared with voltage V_D) at instants in time coinciding with the trailing edge of strobe pulses.

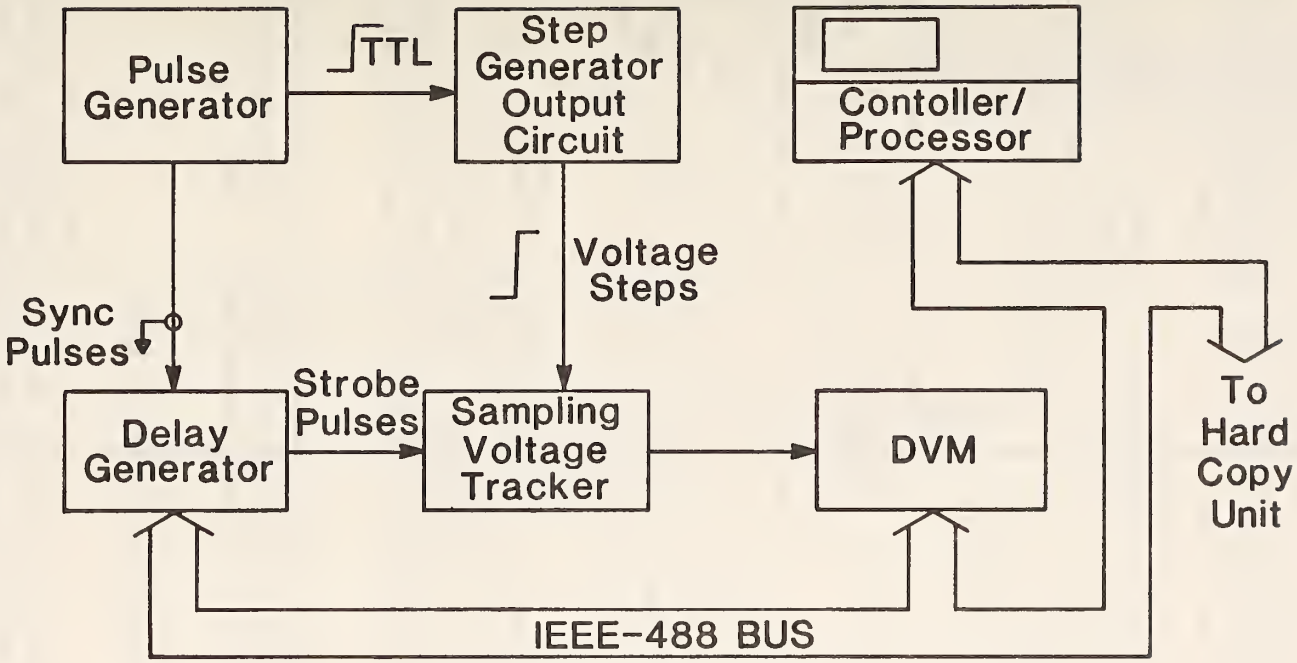


Fig. 7.3 Automatic voltage tracker system used to measure transition characteristics of voltage steps from the step generator.

± 3 V. The TTL pulses applied to the output circuit are delayed 150 ns to approximately match the minimum delay of the delay generator. Figure 7.4 is a plot of a -3 to + 3 V transition of the step generator, when loaded with 30 pF capacitance, a typical input capacitance for waveform recorders. Based on tabulated DVM readings, the transition duration (10-90 percent rise time) was 11 ns and the STs to within ± 0.1 and ± 0.02 percent of FSR were 35 and 39 ns, respectively. When the load capacitance was decreased to 6 pF, the input capacitance of the measuring system, the corresponding STs decreased to 19 and 26 ns. The transition duration decreased to 7 ns. ST measurements, using a peak detector, agreed with the above values to within ± 10 percent.

The peak detector used for negative transitions is shown in figure 7.5. Battery and diode polarities are reversed for positive transitions. The voltage step (applied to the female BNC connector) is adjusted so that the diode conducts during approximately the last 1 percent of the voltage transition. This permits the latter part of a transition to be examined, using a sensitive range of the oscilloscope.

The Schottky diode shown in figure 7.5 has minimum forward conductances of 1 mA and 75 mA at forward voltages of 400 mV and 1 V, respectively. Its shunt capacitance is less than 1 pF. The sensitivity of the detector is calibrated by observing the change in oscilloscope deflection of the upper trace of figure 7.6 caused by a known change in V_A. Since the detector is calibrated using a change in dc voltage, it can also be used to measure very slowly charging voltages such as thermal drift (see section 7.4). The self-heating change of the diode with 0 to 100% duty cycle change causes a computed change in the detector output of 0.05 mV. With a 2 mV/cm scope deflection sensitivity, this corresponds to 0.02 cm deflection change, which is negligible.

Figure 7.6 shows a ST measurement of a 2 V transition from connector L, using a peak detector with negligible input capacitance (~3 pF) and a calibrated sensitivity of 0.25 percent of FSR/cm. The sweep speed was 10 ns/cm. Since the minimum battery voltage is 1.4 V and the diode forward drop is ~0.3 V, the ST of the 2V output was obtained using approximately a 0.3 to + 1.7 V transition.

Deviations from flatness (droop, aberrations, etc.) can be measured to within approximately ± 0.01% of FSR, using a peak detector. This quantity, along with other voltage step limitations are summarized in Table 1 of section 5. SPECIFICATIONS.

7.3 Exponential Waveform Errors

Exponential waveforms having transition durations (risetimes) of 0.55 μs and 27.5 μs are available for dynamic linearity testing of waveform recorders, using external capacitors. The deviation of these waveforms from the true exponential response has been determined using the sampling voltage tracker to measure the waveforms, and then fitting the data to an ideal model of the form $Y = A_0 - A_1 e^{-BT}$ using a nonlinear least-squares curve fitting routine. The maximum values of the residuals of the curve fitting are given in Table 1 of section 5.

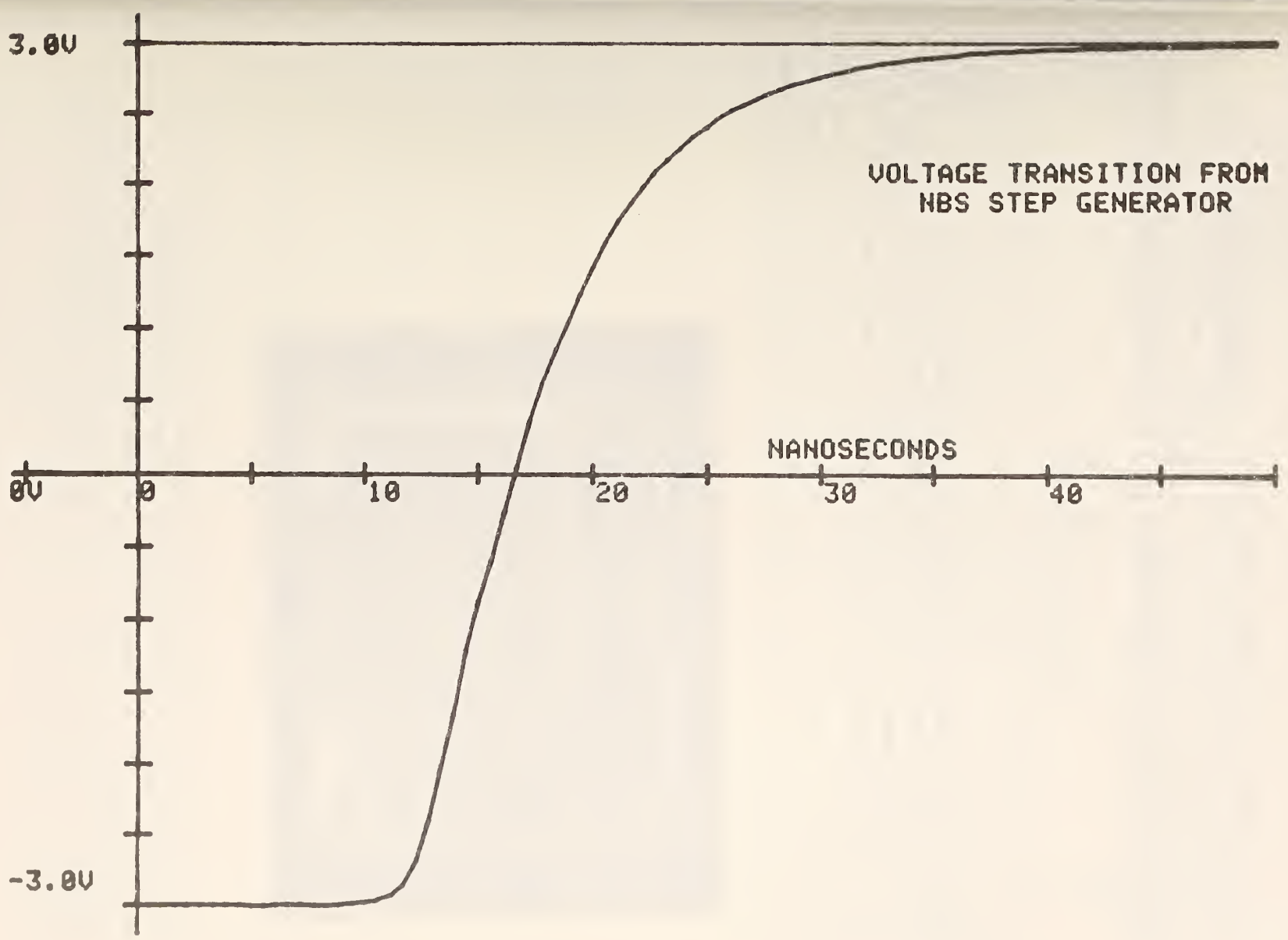


Fig. 7.4 Plot generated by the system shown in figure 7.3 of a -3 to +3 V transition of the step generator, when loaded with 30 pF capacitance.

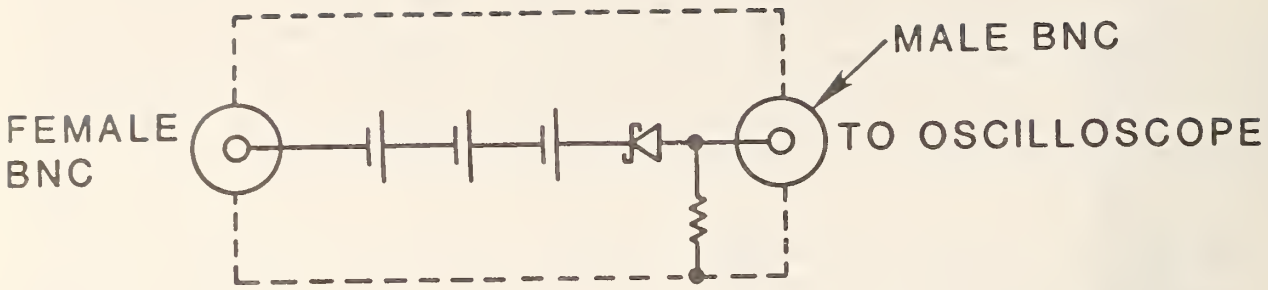


Fig. 7.5 Peak detector using small H_g hearing aid batteries, ~ 1.4 V each. Reverse bias on the diode is determined by the number of batteries employed. Shunt capacitance of the diode is less than 1 pF. The terminating resistance is typically less than 180 Ω.

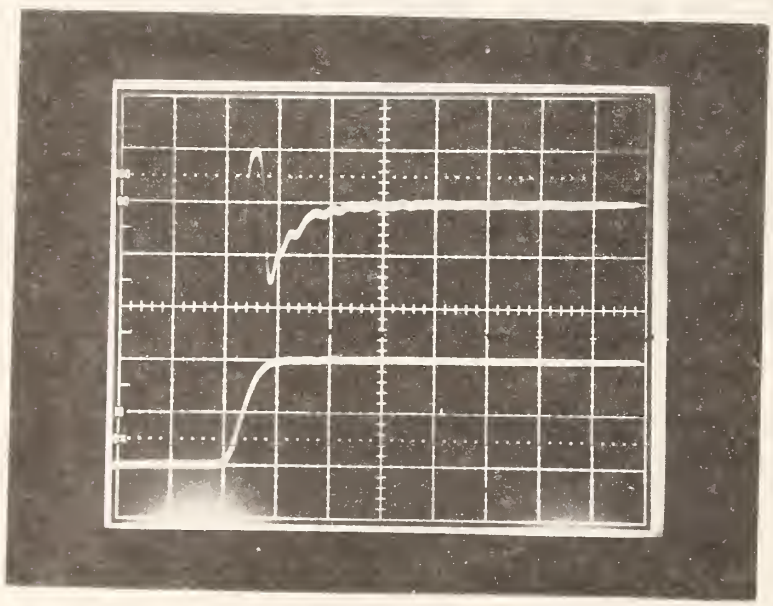


Fig. 7.6 Upper trace shows peak detector response to a +2 V transition of V_L (lower trace). Sweep speed is 10 ns/cm and detector sensitivity is 0.25 percent of 2 V FSR/cm. The initial narrow pulse in detector output is caused by shunt capacitance of the detector diode (see Fig. 7.5). The waveform following this pulse accurately represents the transition of V_L.

The software used to compute these residuals employs an algorithm based on a Gauss-Newton approach [14].

A few practical difficulties are encountered in using the capacitor modules. With the 0.55 μs unit, ringing was significant for approximately the first 50 ns of the transition. With the 27.5 μs unit, some slumping of V_A was encountered during a transition. This effect was minimized by using additional filter capacitance in the output circuit of the step generator (see section 3.1).

7.4 Duty Cycle Dependence

In many high speed circuits, transient thermal imbalances often arise, causing effects such as droop, or "thermal tails", and duty cycle dependence. These effects have been measured for the step generator, using peak detector circuits to discriminate very small changes in the step level following switching. For these measurements, pulse repetition rates ranging from 1 kHz to less than 10 Hz were employed. Changes of less than 0.02 percent in the first 100 ms were noted in the final level when changing the duty cycle between five and ninety five percent, for 10 V steps. The changes increased to a maximum of less than 0.05 percent, after about 30s. For the latter measurement, a single shot step and a scope with a free-running sweep were used (see section 7.2 for detector characteristics).

8. CONCLUSIONS

A precision programmable step generator system, designed for use in automated test systems, has been described. The step generator is intended for testing waveform recorders and digitizing oscilloscopes with resolutions of 8 to 10 bits and bandwidths up to 50 MHz. Fast, accurate settling, together with the programmability of step levels, duty cycles, and repetition rates provides the means for testing the dynamic and thermal characteristics of waveform recorders and digitizing scopes. These characteristics include step response, impulse response, and frequency response; transient characteristics, including dynamic linearity, settling time, transition duration, and transient thermal errors, can also be tested. All voltage levels in the system are also programmable. These levels can be used for static measurements to determine the offset, gain, linearity, and noise of the waveform recorder or digitizing scope under test.

9. ACKNOWLEDGEMENTS

The authors are grateful to P. S. Hetrick for AVT software and calibration assistance, to M. E. Parker for packaging and technician help, and to R. H. Palm for preparation of SG drawings and technician help. They would also like to thank Ms. Y. Dube, Mrs. M. E. Sullivan, and Mrs. B. Meiselman for their help in preparing this report.

10. REFERENCES

[1] T.M. Souders, D.R. Flach, and H.K. Schoenwetter, "Transient Response Characterization of Waveform Recorders," Digest of Technical Papers, 5th IEEE Pulse Power Conference, Arlington, VA, pp. 352-355, June 1985.

[2] H.K. Schoenwetter, "Settling Time Measurements," NBS Special Publication 707, Digital Methods in Waveform Metrology, edited by B.A. Bell, Oct. 1985. (Oct. 1983 Seminar, NBS, Gaithersburg, MD)

[3] J.R. Andrews, B.A. Bell, and E.E. Baldwin, "Reference Flat Pulse Generator," Nat. Bur. Stand. (U.S.) Tech Note 1067, Oct. 1983.

[4] G.J. Frye, "A Predictable Subnanosecond Pulse Generator," IEEE Trans. Instrum. Meas., vol. IM-17, no. 4, pp. 324-329, Dec. 1968.

[5] B.J. Elliott, "Picosecond Pulse Measurement of the Conduction Current Versus Voltage Characteristics of Semiconductor Materials with Bulk Negative Differential Conductivity," IEEE Trans. Instrum. Meas., vol. IM-17, no. 4, pp. 330-332, Dec. 1968.

[6] R.A. Lawton, N.S. Nahman, and J.M. Bigelow, "A Solid State Reference Waveform Standard," IEEE Trans. Instrum. Meas., vol. IM-33, no. 3, pp. 201-205, Sept. 1984.

[7] J.R. Andrews, B.A. Bell, N.S. Nahman, and E.E. Baldwin, "Reference Waveform Flat Pulse Generator," IEEE Trans. Instrum. Meas. vol. IM-32, no. 1, pp. 27-32, Mar. 1983.

[8] H.K. Schoenwetter, "A Programmable Precision Voltage-Step Generator for Testing Waveform Recorders," IEEE Trans. Instrum. Meas., vol. IM-33, no. 3, pp. 196-200, Sept. 1984.

[9] Reference Manual, "4051 GPIB Hardware Support," Part No. 070-2270-00, Tektronix, Inc., Beaverton, OR, Rev. July 1981.

[10] IEEE Std. 488-1978, "IEEE Standard Digital Interface for Programmable Instrumentation," Revision of ANSI/IEEE Std. 488-1975, Institute of Electrical and Electronics Engineers, Inc., 345 East 47th St., New York, NY 10017.

[11] S.P. McCabe III, "A Sampling Voltage Tracker for Analyzing High Speed Waveforms," M.S. Thesis, Univ. CA, Los Angeles, 1975.

[12] R.R. Castleberry and C.L. Robertson, "One-Chip DAC Delivers Composite Video Signal," Electron. Des., pp. 105-112, Sept. 1, 1983.

[13] J. Halpert and M. Koen, "A Waveform Digitizer for Dynamic Testing of High Speed Data Conversion Components," in Dig. 1983 Int. Test Conf., (Philadelphia, PA), Oct. 1983.

[14] "Plot 50, Statistics Volume 4 (Nonlinear Problems)," Tektronix, Inc., Beaverton, OR, 1977.

APPENDIX A

The following paper describes a number of test methods for characterizing waveform recorders, employing the NBS Step Generator in an automated system. This paper is reprinted from the Digest of Technical Papers, 5th IEEE Pulse Power Conference, Arlington, VA, June 1985.

TRANSIENT RESPONSE CHARACTERIZATION OF WAVEFORM RECORDERS

T.M. Souders, D.R. Flach, and H.K. Schoenwetter
Electronic Instrumentation and Metrology
Electrosystems Division
National Bureau of Standards
Gaithersburg, MD 20899

Funded in part by: Sandia National Laboratories

Test methods for characterizing the transient response of waveform recorders are presented, together with typical test results. The methods, based on the use of a precision, programmable step generator developed at NBS, are suitable for recorders having up to 10 bits of resolution and 100 MHz bandwidth.

Introduction

Waveform recorders are subject to a number of types of errors which can limit their ability to accurately characterize transient signals [1, 2, 3, 4]. Principle among these are dynamic linearity errors, impulse response and settling time limitations, transient thermal errors, and time base jitter. An automated measurement system based on a precision programmable step generator has been developed for characterizing such errors in waveform recorders having up to 10-bits of resolution, and bandwidths on the order of 100 MHz.

The test system is designed to output programmable voltage pulses, with one well-defined transition per period, the beginning and terminating levels of which are designated V_1 and V_2. (The transition from V_2 to V_1 is less well characterized, and is not relied upon for most measurements.) Either single shot or repetitive pulses can be generated, with the repetition rate and duty cycle program-mable over many orders of magnitude. The initial and final levels defining the steps are each programmable within the range of ± 1 V for a 50 Ω termination and within ± 5 V for a high impedance load. Voltage steps within these ranges settle smoothly, with no overshoot, to within 0.1% of full scale range in less than 15 and 19 ns, respectively, for small load capacitance. The corresponding 10-90 percent transition durations are approximately 6 ns and 7 ns. The voltage step waveform has been characterized by independent means, and has been shown to approximate a simple exponential response. At high values of output capacitance, the more slowly rising waveform becomes sufficiently close to an ideal exponential that it can be used for dynamic measurements of linearity errors.

System Description

A block diagram of the complete test system is given in figure 1. Overall control is provided via the IEEE 488 bus, for which an internal listener interface has been provided. The waveform recorder under test is also interfaced to the controller via this bus. To minimize load capacitance, the output circuit of the step generator has been designed as a small hand-sized package which connects directly to the input terminals in the same fashion as many sampling heads for sampling oscilloscopes. The generator's power and control signals are provided by a separate support package via a flexible umbilical cable.

A functional diagram of the output circuit of the step generator is shown in figure 2. A more detailed

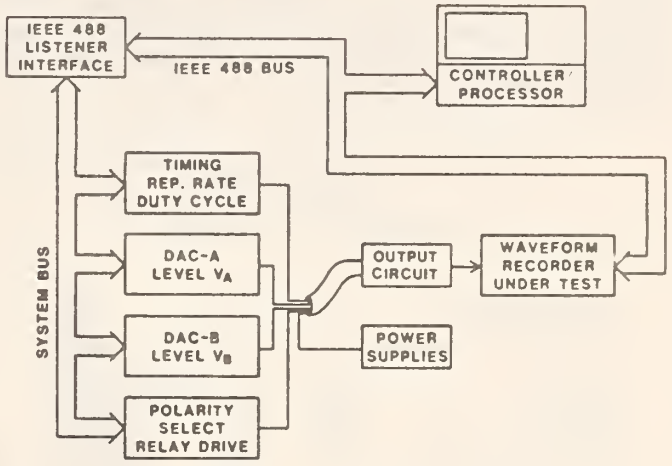


Fig. 1. Block diagram of test system.

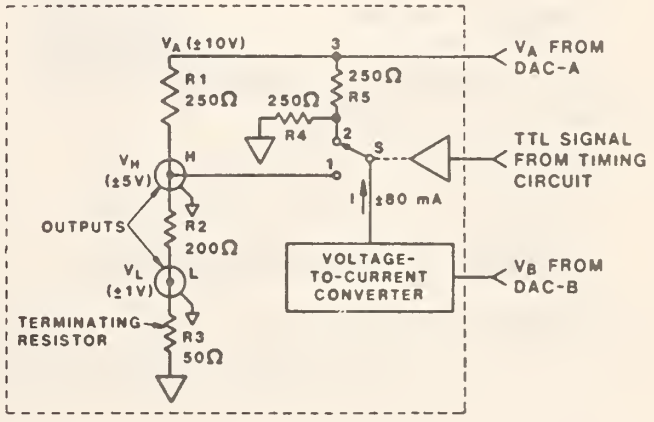


Fig. 2. Simplified diagram of step generator output circuit.

description can be found in reference [5]. Two output ranges are provided: a ±5 V range from output H, intended for high impedance loads, and a ±1 V range from output L for 50 Ω loads. When output L is used, the 50 Ω terminating resistor shown in the figure is actually the input impedance of the test device; otherwise, a 50 Ω coaxial termination is used. The precision step is generated by switching the current source from position 1 to 2. After switching, all active elements are isolated from terminal 1. Consequently, the transition is essentially an exponential waveform determined by the 125 Ω output resistance and the total capacitance between terminal H and ground.

As was previously mentioned, highly accurate exponential waveforms are produced by the generator at higher levels of output capacitance. These waveforms are readily obtained by shunting output terminal H

with high quality capacitors contained in small in-line enclosures which can be connected directly to the output terminal H.

Dynamic Linearity Testing

Exponential waveforms having transition durations of 0.55 μs or longer are available for dynamic linearity testing using external capacitors. The deviation of these waveforms from the true exponential response has been determined using a sampling voltage tracker [6] to measure the waveforms, and then fitting an ideal model of the form $Y = A_1 - A_2e^{Bt}$ to the data using a nonlinear least-squares curve fitting routine. The errors in these waveforms, as indicated by the residuals of the curve fitting process, are less than 0.05% as shown in Table 1.

TABLE 1

Performance Specifications

Static Errors	V_2	V_1	
Offset	0.01	1.0	% FSR
Gain	0.01	1.0	% FSR
Linearity (Max)	0.02	0.5	% FSR
Noise (40 MHz BW)	<500	<500	μV p-p

Step Limitations	±5 V	± 1 V	
Transition Duration	7	6	ns
Settling Time			
0.1%	19	15	ns
0.02%	26	22	ns
Equivalent Bandwidth	50	58	MHz
Droop/Abberations			
After Settling	<0.02	<0.02	% FRS

Exponential Waveforms	0.55 μs	27.5 μs	
Deviation From			
Ideal Waveform (Max)	0.05	0.01	% FSR
rms	0.01	0.006	% FSR

Duty Cycle Dependence		
V_2 Level Change With Duty Cycle (5%-95%)		
0-100 ms	<0.02	% FSR
Max. Final Change (30 s)	<0.05	% FSR

Dynamic linearity measurements are made in the same way by digitizing the exponential waveforms with the recorder under test. Once the waveform has been recorded, the linearity errors are computed from the residuals of the curvefit.

Results of two dynamic linearity tests, one performed on a 10-bit, 60 MHz (sampling rate) recorder and the other on an 8-bit, 200 MHz unit, are presented in figures 3 and 4. The first shows the linearity errors (residuals) of the recorder tested with a waveform having a 27.5 μs transition duration. The maximum and rms errors are 1.5 and 0.42 least significant bits (LSB), respectively. Figure 4 shows the errors with an exponential input having a 0.55 μs transition duration. For this instrument, the maximum and rms errors are 1.3 and 0.46 LSB. In both cases, the ideal maximum and rms error limits are 0.5 and 0.29 LSB, respectively.

Dynamic linearity measurements of this type include errors resulting from ideal quantization uncertainty and time base jitter, as well as differential and integral linearity errors.

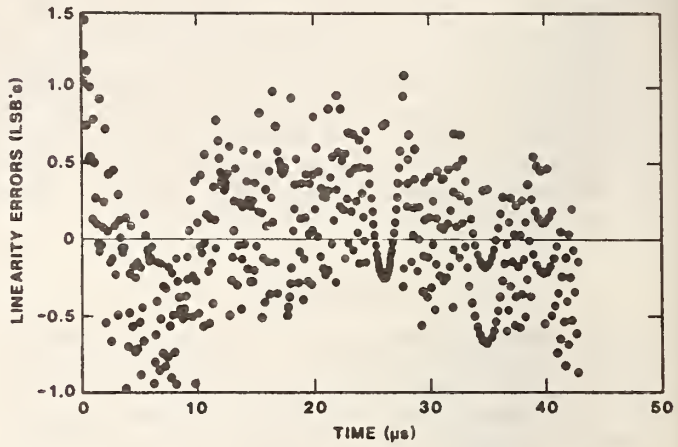


Fig. 3. Dynamic linearity errors of 10-bit, 60 MHz recorder with exponential input signal having 27.5 μs transition duration.

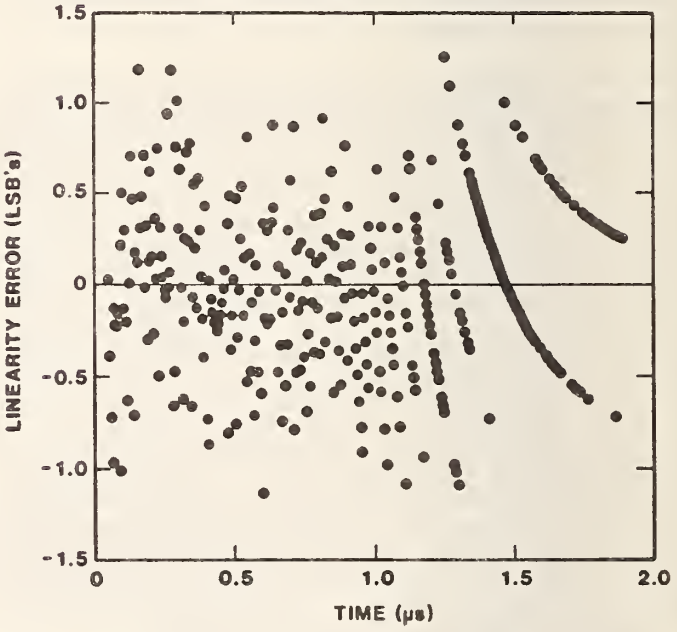


Fig. 4. Dynamic linearity errors of 8-bit, 200 MHz recorder with exponential input signal having 0.55 μs transition duration.

Step Response Measurements

Measurements of step, inpulse, and frequency response, as well as transition duration and settling time can, in principle, all be made directly using the step generator, simply by recording the response to a step, and calculating the desired parameters from the recorded data. In practice, however, two points must be taken into consideration. First, the sampling rate of the test recorder limits the effective bandwidth of the measurement. Because of aliasing errors which result when using a wideband input step, this limitation makes it impossible to characterize the

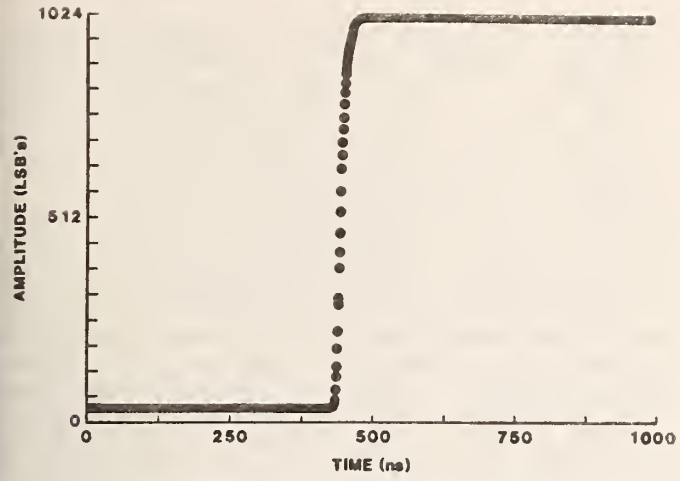


Fig. 5. Step response of 10-bit, 60 MHz recorder, measured using equivalent time method (0.98 ns / sample).

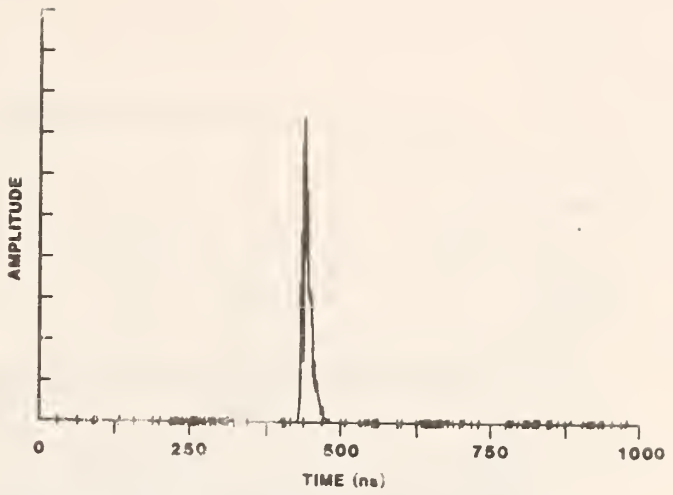


Fig. 6. Impulse response calculated from step response data of figure 5.

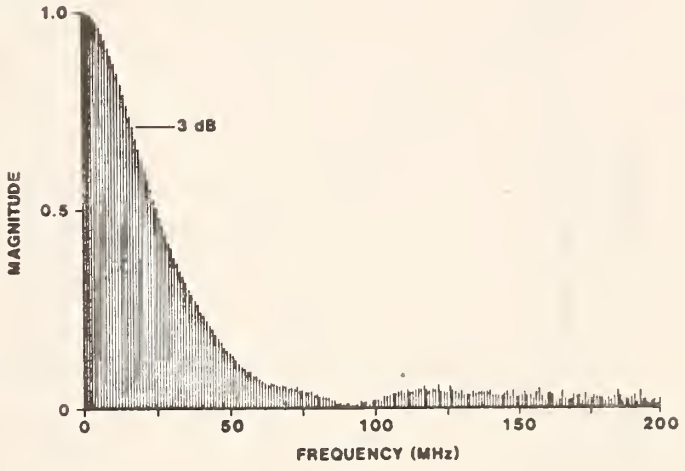


Fig. 7. Frequency response calculated from impulse response data of figure 6. The bandwidth (3 dB point) thus measured is 17 MHz vs. 15 MHz claimed by the manufacturer.

frequency response with reasonable accuracy. The second point is that the input step itself has finite equivalent bandwidth (see Table 1), and for very fast recorders, its frequency response may not be flat enough to ignore.

The sampling rate limitation can often be overcome by extracting equivalent time sampling data from a single record, provided that the repetition rate of the input step is selected appropriately, as follows. Set the ratio of the sample rate, f_s, to the step repetition rate f_r, so that $(N-1) < (f_s/f_r) < N$, where N is some integer, thus not allowing f_s and f_r to be phaselocked.

With the step generator, this is accomplished using an external, programmable frequency synthesized source. If, under these conditions, every Nth sample is taken from the record of length M, then the resulting M/N data points will represent equivalent time samples of the original waveform. The exact repetition rate needed to obtain one complete period sampled in equivalent time can be calculated, given a choice of N, from

$$f_r = (f_s / N)\ (N/M + 1).$$

Note that N/M is the reciprocal of the number of samples that will be in the final record, so that this ratio determines the number of equivalent time samples in one period of the input step. It can be seen from this relationship that the measurement bandwidth is directly proportional to the record length. The interval between the equivalent time samples is given by

$$\Delta t = N(1/f_s - 1/Nf_r).$$

Problems imposed by the limited bandwidth of the step generator can be overcome to some extent, by mathematically deconcolving its response from the recorded response of the waveform recorder under test [7]. The ability to accurately measure the input step using independent, equivalent time techniques makes it possible to at least double the effective bandwidth of measurements made with the step generator. In a future paper, the application and results of deconvolution techniques will be presented.

Some typical test results are given in figures 5-8 for a 10-bit, 60 MHz recorder. These plots give, in order, recorded step response, impulse response, frequency response (showing the computed 3 dB point at 17 MHz), and settling with apparent undershoot of approximately 8 LSBs. Equivalent time sampling was used for all measurements except settling time, with an equivalent sampling interval of 0.98 ns.

To illustrate the utility of such data in predicting the response of a particular waveform recorder when digitizing real-world signals, figure 9 presents an example in which a double exponential waveform is considered. The figure shows an ideal waveform (0.125/10 μs rise/fall time) together with the response error predicted by convolving it with the measured impulse response. Distortion, causing error in the peak value on the order of 7 LSBs, is plotted in figure 9-b. To arrive at an overall estimate of the errors which would likely occur when digitizing such a candidate waveform, the dynamic linearity errors, as presented in figure 3, should also be included.

Testing of Transient Thermal Response

It is common practice to calibrate waveform recorders using static measurement methods. These data are used, if deemed necessary, to correct the actual data obtained when transient waveforms are recorded. In fact, such a process is used in the self calibration

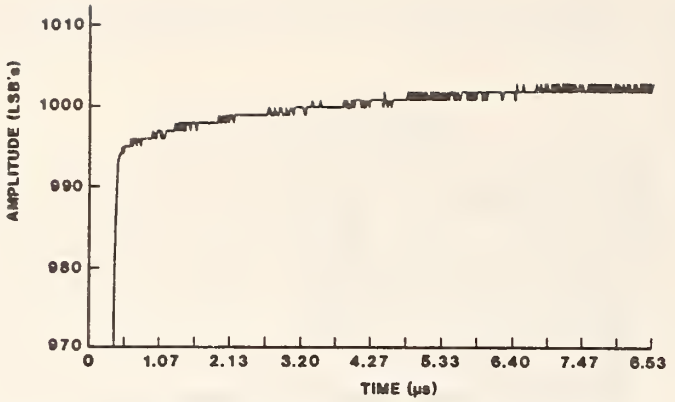


Fig. 8. Expanded view of step response of 10-bit, 60 MHz recorder, showing 8 LSB undershoot and settling time of approximately 6 μs to 1 LSB.

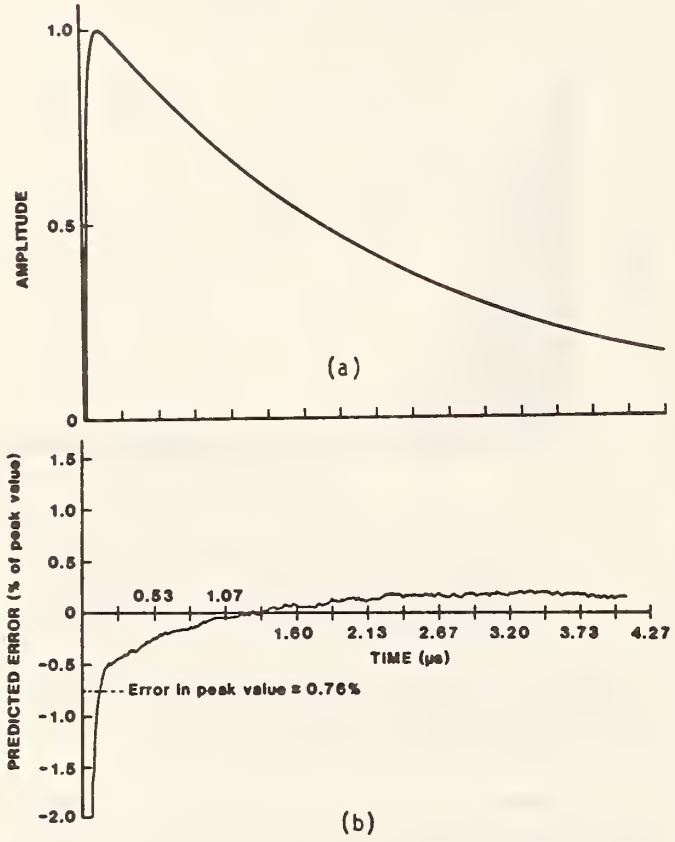


Fig. 9. Ideal double exponential input waveform with 0.125/10 μs rise/fall time (a), and predicted response error (b).

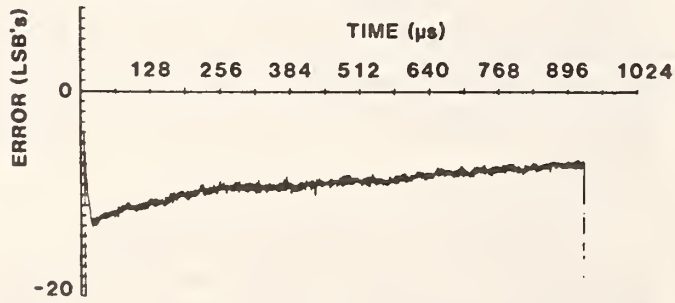


Fig. 10. Transient thermal response of 10-bit, 20 MHz recorder.

routines of several commercial recorders. Unfortunately, even for very slow events, the waveform recorder will likely respond differently to transient signal levels than to dc levels, primarily because of internal transient thermal imbalances which can have rather long time constants. Because these effects are related to signal power, they are nonlinear and thus cannot be represented simply by a transfer function. The magnitude of these effects are easily measured with the step generator however, by first recording one half cycle of a low frequency square wave, and then subtracting from it the record of a dc signal having the same value as the recorded level of the square wave. If transient thermal errors are present, they will appear in the resulting difference between the two records. Figure 10 shows the results of such a test in which a 500 Hz square wave of nearly full scale amplitude has been used. The recording of the upper level of the square wave has been subtracted from a recording of the equivalent dc level. Note the initial overshoot of about 30 μs duration, followed by the long, slowly decaying tail. The peak errors are 12 LSBs.

Conclusions

The step response test system that has been described is capable of accurately measuring many error parameters that are important in assessing the overall transient response of waveform recorders. Fast, accurate settling, together with the programmability of step levels, duty cycles, and repetition rates provides the means needed to measure and separate both linear and nonlinear effects, and to provide information relevant to both the time and frequency domains.

Additional work under way in this area includes the development of a faster generator test head, with a goal of a 2 ns transition duration and settling to 0.1% in 8 ns. This capability would permit the measurement of 10-bit recorders having bandwidths as high as 350 MHz.

References

[1] D. R. Flach, "Steady-State Tests of Waveform Recorders," NBS Special Publ. 643, June 1982.

[2] B. E. Peetz, "Dynamic Testing of Waveform Recorders," IEEE Trans. Instrum. Meas., vol. IM-32, March 1983.

[3] R. A. Malewski, T. R. McComb, and M. M. C. Collins, "Measuring Properties of Fast Digitizers Employed for Recording HV Impulses," IEEE Trans. Instrum. Meas., vol. IM-32, March 1983.

[4] K. Schon, H. Korff, and R. Malewski, "On the Dynamic Performance of Digital Recorders for HV Impulse Measurement," Fourth International Symposium on High Voltage Engineering, paper 66.05, Athens, September 1983.

[5] H. K. Schoenwetter, "A Programmable Precision Voltage-Step Generator for Testing Waveform Recorders," IEEE Trans. Instrum. Meas., vol. IM-33, no. 3, September 1984.

[6] S. P. McCabe III, "A Sampling Voltage Tracker for Analyzing High Speed Waveforms," M. S. Thesis, U. of CA, 1975.

[7] N. S.Nahman and M. E. Guillaume, "Deconvolution of Time Domain Waveforms in the Presence of Noise," Nat. Bur. Stand. (U.S.) Tech. Note 1047.

APPENDIX B

Appendix B contains the documentation for the VSG driver program. This program is written in the Hewlett-Packard BASIC 3.0 language. Pages 60 through 68 contain the program listing. A brief description of each numeric variable is given in pages 69 to 71, and a brief description of each string variable is given on pages 71 and 72. The line labels used in the program are listed on pages 72 through 74, with a short description of the function performed when that section of the program is executed. If a line label is executed when a softkey is pressed, this is indicated by the key number in brackets below the line label. Pages 75 through 87 contain flow charts for each of the defined softkeys and for GOSUB 2500, the main routine used to calculate digital code for the DACs on the DAC/OA board.

Appendix B

VSG Driver Program

```
1 REM DRF VSGDRIVER; 07/15/86; DISC D, NATIONAL BUREAU OF STANDARDS
2 Start:     ! Program remains in a loop at line 80, label Loop
3 OFF KEY
10 ON KEY 0 LABEL "INITALIZE" GOSUB Init  ! Initalize the support unit
14 ON KEY 2 LABEL "TRS,V2,V1" GOSUB Trvls ! Set transition, initial, final level
18 ON KEY 3 LABEL "VSG  freq" GOSUB Vsgfreq  ! Set repetition rate of VSG
22 ON KEY 4 LABEL "PULSE LENGTH  " GOSUB Pulse_length  ! Set pulse duration
26 ON KEY 5 LABEL "DELAY LINE" GOSUB Delayline   ! Set duration with delay line
30 ON KEY 6 LABEL "INTEGER" GOSUB Integer  ! Set Pulse_int and Freq_int
34 ON KEY 7 LABEL "FUNCTIONS" GOSUB Card   ! Displays functions on timing card
38 ON KEY 8 LABEL "ENTER C1,C2" GOSUB C1c2 ! Enter timing control characters
42 ON KEY 9 LABEL " Menu 2 " GOTO Menu2    ! To next menu
44 ON KEY 10 GOSUB Status   ! Display status of VSG parameters
46 ON KEY 11 GOSUB Changetr ! Switch transition, voltage levels remain same
50 ON KEY 12 GOSUB Ckon_off ! Cycle clock ON/OFF or OFF/ON
52 ON KEY 13 GOSUB Ch_f_vl  ! Enter new final voltage level
54 ON KEY 14 GOSUB Ch_i_vl  ! Enter new initial voltage level
80 Loop:   GOTO Loop        ! Program remains here until a Soft Key is pressed
90 PAUSE
100 Init:          ! setup voltage step generator parameters: Frequency= 50 KHz,
105                ! pulse length 50 periods (5.0 uS)
110 Vsg=70812      ! IEEE-488 address of vsg support unit
115 REM
120 CLEAR Vsg      ! Used to reset chip address counter to zero, must always be
121                ! executed before sending new data strings to the boards.
122                ! In this program, it is normally executed after a command
123                ! string is sent
125 OUTPUT Vsg;"12"   ! Turn the clock off
130 CLEAR Vsg         ! Chip address counter to zero
135 Clear_crt$=CHR$(255)&CHR$(75)    ! Used to clear CRT screen
140 REM
145 REM
150 REM Set frequency to Freq/100 (100 KHz), pulse length 50 periods
155 OUTPUT Vsg;"10AC9FFDCFF"   ! Timing board string
160 CLEAR Vsg                  ! Chip address counter to zero
165 OUTPUT Vsg;"10";  ! Clock on
170 CLEAR Vsg
174 OPTION BASE 1     ! Lower bound of arrays is one
175 DIM Bindac_b$[3],Bindac_a$[3],X$[3],Dac$[7],Time$[11]
185 RESTORE 190
190 DATA -1,1,1,"0666C3C"  ! Data for initalization
195 DATA "XXX","10AC9FFDCFF",1,"666","C3C",100,50
200 READ Init_vl,Final_vl,Tr,Dac$,X$,Time$,Tr,Bindac_a$,Bindac_b$
210 READ Freq_int,Pulse_int
225 REM Set positive transition
230 GOSUB Pos_tr
```

```
235 REM Set initial level -1 volt, final level +1 volt
240 OUTPUT Vsg;Dac$    ! Word string to DAC/OA board
245 CLEAR Vsg
250 RETURN        ! Exit Init
450 REM
455 REM PRINT "1=+ TR, 2= -TR, 3=NOP, 4=NOP"
460 INPUT "ENTER CONTROL CHARACTER=",Tr  ! Produce a pulse at output of
461 REM Q1, Q2, Q3 or Q4. Only Q1 and Q2 connected to outside
463 IF Tr<1 THEN 460          ! Error check for valid Tr
464 IF Tr>4 THEN 460          !   "     "    "    "   "
465 IF Tr=1 THEN GOSUB Pos_tr    ! Positive transition pulse
470 IF Tr=2 THEN GOSUB Neg_tr    ! Negative transition pulse
475 IF Tr=3 THEN GOSUB Pulse_q3  ! Not connected off the board
480 IF Tr=4 THEN GOSUB Pulse_q4  ! Not connected off the board
485 RETURN        ! Exit subroutine 460
500 Pos_tr: ! Set positive transition on vsg
502 OUTPUT Vsg;"21"
504 CLEAR Vsg
506 OUTPUT Vsg;"20"
508 CLEAR Vsg
510 RETURN        ! Exit Pos_tr
520 Neg_tr: ! Set negative transition on the Vsg
522 OUTPUT Vsg;"22"
524 CLEAR Vsg
526 OUTPUT Vsg;"20"
528 CLEAR Vsg
530 RETURN        ! Exit Neg_tr
540 Pulse_q3: ! NOP, not used, produces a pulse at Q3
542 OUTPUT Vsg;"24"
544 CLEAR Vsg
546 OUTPUT Vsg;"20"
548 CLEAR Vsg
550 RETURN        ! Exit Pulse_q3
560 Pulse_q4: ! NOP, not used, produces a pulse at Q4
562 OUTPUT Vsg;"28"
564 CLEAR Vsg
566 OUTPUT Vsg;"20"
568 CLEAR Vsg
570 RETURN        ! Exit Pulse_q4
600 Card: ! Display functions available on the timing card
610 OUTPUT 2;Clear_crt$; ! Clear CRT screen
615 PRINT "     ***************TIMING CARD FUNCTIONS*****************"
620 PRINT "CTRL CHARACTER        FUNCTION SELECTED"
625 PRINT "   C1=0              INTERNAL CLOCK"
630 PRINT "   C1=1              EXTERNAL CLOCK"
635 PRINT "   C2=0              PROG. FREQ & PULSE LENGTH"
640 PRINT "   C2=4              OUTPUT FREQ. DIVIDER COUNTERS"
645 PRINT "   C2=12             PULSE LENGTH SET BY DELAY LINE KEY # 5"
650 PRINT "C1=1,C2=4           INITIAL LEVEL OUTPUT "
655 PRINT "C1=1,C2=8           FINAL LEVEL OUTPUT"
660 PRINT "C1=2,C2=0           TURN CLOCK OFF"
662 C1c2: ! Enter C1 & C2 without displaying timing card menu
665 INPUT "ENTER CONTROL CHARACTERS C1,C2",C1,C2
670 REM PRINT C1,C2
```

```
675 C3=C1+C2   ! Compute character for digit 2 in Time$. This is a Hex digit
680 Xx$=IVAL$(C3,16)
681 PRINT Time$   ! Word string for Timing board
682 PRINT Xx$     ! Value of C3 in Hex
685 Time$=Time$[1;1]&Xx$[4]&Time$[3]
686 PRINT Time$   ! Word string for Timing board output to support unit
690 OUTPUT Vsg;Time$ ! Starts new function defined by C1 and C2
695 CLEAR Vsg
700 RETURN  !  Exit Card or C1c2:
725 Ckon_off: ! Cycle  clock ON/OFF or OFF/ON
730 Ck$=Time$[2;1] ! Hex digit in position 2 contains the clock ctrl bit
735 Pos=IVAL(Ck$,16)
740 REM  Complement the clock ctrl bit (2nd bit) in position 2
745 Pos1=BINEOR(Pos,2)
750 Ck$=IVAL$(Pos1,16) ! Hex digit 4 contains new clock ctrl bit
755 Time$=Time$[1;1]&Ck$[4]&Time$[3]
760 OUTPUT Vsg;Time$          ! New word string to Timing board
765 CLEAR Vsg
775 RETURN  ! Exit Ckon_off
1500 Ck_off: ! Turn clock off if on, do not change other bits in position 2
1505 Ck_on$=Time$[1;2]  ! Save for clock turn on
1510 Ck1$=Time$[2;1]    ! Get clock control character
1520 Ck1ctrl=IVAL(Ck1$,16)
1530 Ck2$=IVAL$(Ck1ctrl,2)       ! Bit 15 contains the clock control bit
1540 IF Ck2$[15;1]="1" THEN 1600 ! Clock off, no action required
1550 Ck2ctrl=BINEOR(Ck1ctrl,2)   ! Complement the clock control bit
1560 Ck2$=IVAL$(Ck2ctrl,16)    ! Clock control hex character with clock bit off
1570 Ck3$="1"&Ck2$[4]          ! Assemble string
1580 OUTPUT Vsg;Ck3$;  ! Turn clock off, string sent to Timung board
1590 CLEAR Vsg
1600 RETURN       ! Exit Ck_off
2000 Trvls:  ! Set transition, initial, final voltage level
2010 REM DAC Va with amplifier Ua; -11/+11 volts; Ctrl=1 Gain
2020 REM DAC Vb with amplifier Ub; -20/+20 volts; Ctrl=2 Offset
2030 REM Tr=1 positive transition; Tr=2 negative transition
2040 REM ENTER TRANSITION, FINAL, INITIAL VOLTAGE LEVEL
2050 INPUT "ENTER Tr, Final_vl, Init_vl=",Tr,Final_vl,Init_vl
2060 IF Tr=1 OR Tr=2 THEN 2100    ! Valid entry for transition when true
2075 BEEP 200,.2
2080 PRINT "Tr=";Tr;" IS ILLEGAL ENTRY, Tr=1 IS + TRANS, Tr=2 IS - TRANS"
2090 GOTO Trvls  ! Reenter the transition
2100 Final_vlrg: ! Check range of final voltage level for +/- transition
2110 IF Final_vl<=-4.9975585 OR Final_vl>4.9975585 THEN 2130
2120 GOTO 2200       ! This line executed when voltage valid
2130 REM Final voltage range error statement
2140 BEEP 200,.3
2150 PRINT "FINAL VOLTAGE LEVEL= ";Final_vl;" VOLTS IS OUT OF RANGE"
2160 PRINT "FINAL VOLTAGE RANGE IS -4.9975585 TO +4.9975585 VOLTS"
2170 GOTO 2040  ! Final voltage level not valid, reenter another value
2200 Init_vlrg: ! Check range of initial voltage level for +/- transition
2210 IF Tr=1 THEN 2250 ! Check range of initial voltage level for + transition
2220 IF Tr=2 THEN 2350 ! Check range of initial voltage level for - transition
2250 REM Positive transition, initial voltage level check
2260 IF Init_vl>=Final_vl THEN 2290  ! Invalid voltage when true
```

```
2270 IF Init_vl<-4.9975585 THEN 2310 ! Invalid voltage when true
2280 GOTO 2430 ! Passed all voltage checks, compute DAC codes, etc.
2290 PRINT "INITIAL VOLTAGE LEVEL>= FINAL LEVEL NOT ALLOWED ON + TRANSITION"
2295 BEEP 200,.3
2300 GOTO 2040 ! Voltage levels not valid, enter new ones
2310 PRINT "INITIAL VOLTAGE=";Init_vl;" IS < -4.9975585 VOLTS,  OUTSIDE OF RANGE
"
2315 BEEP 200,.2
2320 GOTO 2040 ! Voltage levels not valid, enter new ones
2350 REM  Negative transition, initial voltage level check
2355 IF Init_vl>4.9975585 THEN 2410   ! Invalid voltage when true
2360 IF Init_vl<=Final_vl THEN 2390   ! Invalid voltage when true
2380 GOTO 2500 ! Passed all voltage checks, COMPUTE dac codes, etc.
2390 PRINT "INITIAL VOLTAGE <= FINAL VOLTAGE LEVEL NOT ALLOWED ON - TRANS."
2395 BEEP 200,.2
2400 GOTO 2040 ! Voltage levels not valid, enter new ones
2410 PRINT "INITIAL VOLTAGES > 4.997585 ARE OUTSIDE OF RANGE"
2415 BEEP 200,.2
2420 GOTO 2040   ! Voltage levels not valid, enter new ones
2430 REM         ! End of voltage level checks
2440 GOSUB 2500  ! To output of the voltages
2450 RETURN      ! Exit Trvls
2500 Dacv_s: ! Compute voltages and binary codes needed for DAC Va & Vb outputs
2510 GOSUB 2800  ! DAC Vb voltages and code calculations
2520 GOSUB 2900  ! DAC Va voltage and code calculation
2530 REM Compute DAC codes
2540 REM  GOSUB 3000 ! Can be used as an entry if Ctrl is set for calculating a
2541 REM DAC VOLTAGE
2550 PRINT "Init_vl= ";Init_vl
2560 PRINT "Final_vl =";Final_vl
2570 GOSUB 1500  ! Turn clock off
2580 OUTPUT Vsg;Dac$      ! Output new Va and Vb voltages
2590 CLEAR Vsg
2600 OUTPUT Vsg;Ck_on$;   ! Turn clock on
2610 CLEAR Vsg
2620 IF Tr=1 THEN GOSUB 500  ! Set positive transition
2630 IF Tr=2 THEN GOSUB 520  ! Set negative transition
2633 PRINT Dac$   ! String sent to DAC/OA board
2640 RETURN       ! Exit Trvls
2800 Dac_vb:      ! DAC Vb voltage calculation
2810 REM Output at amplifier Ub, -20/+20 volts, Ctrl = 2
2820 Xdacb=-SGN(Final_vl-Init_vl)*(ABS(Final_vl-Init_vl)+8.3) ! Mult by -0.5
2821 REM for DAC Vb output voltage
2830 Xdacb1=-.5*Xdacb   ! Save if needed later
2840 Vdac=-.5*Xdacb     ! Voltage for DAC code calculation
2850 Ctrl=2             ! DAC Vb calculations
2860 GOSUB 3000         ! Do DAC code calculations
2870 RETURN  ! Exit Dac_vb
2900 Dac_va: ! DAC Va voltage calculation
2910 REM Output at amplifier Ua of -11/+11 volts
2920 Ydaca=1.818181*Final_vl  ! DAC A OUTPUT V
2930 Ydaca1=-Ydaca  ! Save IF NEEDED LATER
2935 Vdac=-Ydaca    ! Voltage for DAC code calculation
2940 Ctrl=1         ! DAC Va calculations
```

```
2950 GOSUB 3000      ! DAC code calculation
2960 RETURN    ! Exit Dac_va
3000 Code: ! Compute complementary offset binary codes for the 12 bit DAC'S
3010 REM Entry voltage is variable Vdac
3020 REM Ctrl= 2 for DAC Vb w/ Ub output +/- 20 volts
3030 REM Ctrl= 1 for DAC Va w/ Ua output +/- 11 volts
3040 REM
3050 Vdac3=Vdac+10    ! Add 10 volt offset so no minus values
3060 Lsb_s=Vdac3*204.8+.4999999  ! Put Vdac3 in LSB's of a 12 bit DAC
3062 IF Ctrl=1 THEN Raw_lsb_1=Lsb_s     ! Save for use in removing digitizing
3063 IF Ctrl=2 THEN Raw_lsb_2=Lsb_s     ! digitizing errors
3070 Lsb_s=INT(Lsb_s)                   ! Digitize Vdac3
3090 REM Convert LSB's to Hex code
3100 Hex1$=IVAL$(Lsb_s,16)
3110 X$=Hex1$[2]   ! Use first 3 Hex digits (12 bit DAC's)
3115 X$=REV$(X$)  ! Reversal of digits needed  to match DAC registers
3120 IF Ctrl=1 THEN GOSUB Bindaca    ! Binary code for DAC Vb
3130 IF Ctrl=2 THEN GOSUB Bindacb    ! Binary code for DAC Va
3140 RETURN    ! Exit Code
3150 Bindacb: ! Binary code for DAV Vb, Ctrl=2
3157 V$=X$
3158 V$=TRIM$(V$)
3160 Bindac_b$=X$
3170 Dac$="0"&Bindac_a$&V$    ! Assemble string for DAC/OA board
3180 RETURN    ! Exit Bindacb
3200 Bindaca: ! Binary code for DAC Va, Ctrl=1
3210 Bindac_a$=X$
3220 Dac$="0"&Bindac_a$&V$    ! Assemble string for DAC/OA board
3222 PRINT Dac$;"DAC A"
3230 RETURN    ! Exit Bindaca
4000 Vsgfreq: ! Enter Vsg drive  frequency based on 10 MHz internal clock
4010 PRINT "CLOCK  FREQUENCY RANGE 153 TO 3.333 MHZ WITH 10 MHZ INTERNAL CLOCK"
4011 PRINT "HIGHEST SQUARE FREQUENCY IS 2.5 MHZ WITH INTERNAL CLOCK"
4020 INPUT "ENTER VSG DRIVE  FREQUENCY IN HZ",Vsgfreq1
4030 REM Vsgfreq1 is user entered frequency, calculations below for closest
4031 REM frequency system can output. Clock frequency is divided by an integer
4032 REM to produce the Vsg drive frequency.
4040 Freq_int=INT((10000000/Vsgfreq1)+.4999999)    ! Closest Vsg drive freq
4041 REM positive integer to the user entered freq. INT/EXT clock divided by
4042 REM this integer. Minimum value can be entered is 3
4050 IF Pulse_int>=Freq_int THEN 4090 ! Go to error statement
4060 PRINT "CLOSEST Vsg FREQUENCY IS ";10000000/Freq_int
4070 REM
4080 GOTO 4200 ! Passed error statements, output freq to Vsg
4090 REM Error statement, pulse length > Vsg freq
4095 BEEP 200,.2
4100 PRINT "PULSE LENGTH TOO LONG FOR Vsg FREQUENCY"
4110 PRINT "PULSE LENGTH=";Pulse_int;" PERIODS"
4120 PRINT "MAX Vsg FREQUENCY=";(10000000/(Pulse_int+1))
4130 GOTO 4010 ! Reenter the Vsg frequency
4140 REM Divide the INT/EXT clock frequency by an integer to find Vsg drive
4141 REM frequency
4150 REM Max integer is 65535, positive values only
4160 REM Time$= "10YXXXXGGGG"
```

```
4170 REM No error statement in this routine
4180 INPUT "INT/EXT CLOCK FREQ DIVISOR (INTEGER, MAX= 65535)= ",Freq_int
4190 REM
4200 REM Target from 4080, do calculations to output Vsg freq
4210 REM
4220 Freq_int2=65536-Freq_int ! Put in format to load registers in support unit
4230 OUTPUT Vsg;"12";   ! Turn clock off
4240 CLEAR Vsg
4250 F$=DVAL$(Freq_int2,16)  ! Compute string for Timing board
4251 F$=F$[5]     ! Last 4 digits contain the clock digits
4260 F$=REV$(F$)  ! Formatting for output to registers
4270 Time$=Time$[1;3]&F$&Time$[8]   ! Assemble string for Timing board
4280 OUTPUT Vsg;Time$        ! Output to Timing board
4290 CLEAR Vsg
4300 RETURN   ! Exit Vsgfreq:
5000 Pulse_length:  ! Set pulse length with 10 MHz internal clock
5010 REM  Pulse length is duration of final voltage level
5020 INPUT "ENTER PULSE LENGTH IN NANOSECONDS (UNITS OF 100)=",Plength
5030 Pulse_int=INT((Plength+49.99999)/100)-1 ! To nearest 100 nS; -1 added for
new timing board (10-Jul-86)
5040 IF Pulse_int>=Freq_int THEN 5070   ! To error statement
5050 Pulse_int2=65536-Pulse_int  ! Format for the output registers
5060 GOTO 5170 ! To output pulse length to Vsg
5070 REM Error statement, pulse length > clock frequency
5075 BEEP 200,.2
5080 PRINT "PULSE LENGTH TOO LONG FOR CLOCK FREQUENCY"
5090 PRINT "FREQUENCY=";10000000/Freq_int
5100 REM
5110 PRINT "MAXIMUM PULSE LENGTH=";(Freq_int-1)*100;" NANOSECONDS"
5120 GOTO 5020  ! Reenter the pulselength
5130 REM Enter the length of the pulse < freq division
5140 REM Pulse length = integer*clock period
5160 REM
5170 Pulse_int2=65535-Pulse_int   ! Format for timing board registers
5180 OUTPUT Vsg;"12"; ! Turn clock off
5190 CLEAR Vsg
5200 P$=DVAL$(Pulse_int2,16)      ! Compute the Timing board string
5201 P$=P$[5]     ! Last 4 digits contain the pulse length information
5210 P$=REV$(P$) ! Reverse the digits to match the timing board registers
5220 Time$=Time$[1;7]&P$      ! Assemble Timing board string
5230 OUTPUT Vsg;Time$        ! Output to timing board
5240 CLEAR Vsg
5250 RETURN   ! Exit Pulse_length:
5500 Integer: ! Enter the pulse length & Vsg drive with positive integers
5510 INPUT "FREQ DIVISOR, PULSE LENGTH CLOCK PERIODS",Freq_int,Pulse_int
5520 Freq_int=INT(Freq_int)   ! Minimum value is +3
5530 Pulse_int=INT(Pulse_int) ! Minimum value is +1
5531 Pulse_int=Pulse_int-1    ! Needed for new timing board (15-JUL-86) the
5532                          ! minus one
5540 IF Pulse_int>=Freq_int THEN     ! To error statement if true
5550 BEEP 200,.2
5560 PRINT "ERROR! FREQ DIVISOR <= CLOCK PERIOD, MUST BE >"
5570 GOTO 5510    ! Enter new pulse length
5580 END IF
```

```
5590 GOSUB 5170 ! Enter pulse length
5600 GOSUB 4220 ! Enter Vsg drive freq
5610 RETURN     ! Exit Integer :
6000 Delayline: ! Set pulse length with programmable delay line
6001 IF Pulse_int<2 OR Freq_int<3 THEN    ! Error condition if true for P.D.L.
6002 PRINT "PULSE LENGTH MUST BE GREATER THEN 1 CLOCK PERIOD WHEN USING"
6003 PRINT "PROGRAMMABLE DELAY LINE AND CLOCK FREQUENCY DIVISOR GREATER THEN 3"
6004 BEEP 200,.2
6005 GOTO 6070  ! Execute return, need to change timing board parameters
6006 END IF
6010 PRINT "PULSE LENGTH IS PROGRAMMABLE IN 16 TEN NANOSECOND STEPS 1-16"
6020 INPUT "STEP SIZE  1 TO 16=",Delay_line
6030 Xx1$=IVAL$(Delay_line-1,16) ! Subtract one so range is one Hex digit
6040 Time$=Time$[1;2]&Xx1$[4]&Time$[4] ! Last digit of Xx1$ contains P.D.L. code
6050 OUTPUT Vsg;Time$        ! Output delay line data to Timing board
6060 CLEAR Vsg
6070 RETURN  ! Exit Delayline
6400 Status: ! Print out the current Vsg system parameters
6410 OUTPUT 2;Clear_crt$;
6420 PRINT "++++++++++++++ CURRENT VSG PARAMETERS ++++++++++++++++++++++"
6430 SELECT Time$[2;1] ! Print out the current function on the timing card
6440 CASE "0"
6450 PRINT "INTERNAL CLOCK ON"
6460 PRINT "PULSE LENGTH SET USING PROGRAMMABLE COUNTERS"
6470 CASE "1"
6480 PRINT "EXTERNAL CLOCK ON"
6490 PRINT "PULSE LENGTH SET WITH PROGRAMMABLE COUNTERS"
6500 REM
6510 CASE "2"
6520 PRINT "TURN INTERNAL/EXTERNAL CLOCK OFF"
6530 REM
6540 CASE "5"
6550 PRINT "INTERNAL/EXTERNAL CLOCK OFF"
6560 PRINT "OUTPUT SET AT INITIAL LEVEL"
6570 CASE "9"
6580 PRINT "INTERNAL/EXTERNAL CLOCK OFF"
6590 PRINT "OUTPUT SET AT FINAL LEVEL"
6600 CASE "C"
6610 PRINT "INTERNAL CLOCK ON"
6620 PRINT "PULSE LENGTH SET BY DELAY LINE"
6630 D=IVAL(Time$[3;1],16)
6640 PRINT "PULSE LENGTH=";(D+1)*10;" NANOSECONDS"
6650 CASE "D"
6660 PRINT "EXTERNAL CLOCK ON:"
6670 PRINT "PULSE LENGTH SET WITH DELAY LINE"
6680 D=IVAL(Time$[3;1],16)
6690 PRINT "PULSE LENGTH=";(D+1)*10;" NANOSECONDS"
6700 END SELECT
6710 PRINT "USE OF KEY 12 (Ckon_off) MAKES CLOCK ON OR OFF INDETERMINATE"
6720 PRINT "VOLTAGE STEP GENERATOR REPETITION RATE=";10000000/Freq_int;
6730 PRINT " HZ"
6740 PRINT "PULSE LENGTH=";(Pulse_int+1)*100;" NANOSECONDS IF PROGRAMMABLE"
6750 PRINT "COUNTERS IN USE"
6760 Tr$="POSITIVENEGATIVE"
```

```
6770 PRINT Tr$[(Tr-1)*8+1;8];" TRANSITION"
6780 PRINT "FINAL LEVEL =";Final_vl;" VOLTS"
6790 PRINT "INITIAL LEVEL =";Init_vl;" VOLTS"
6800 PRINT "     IF EXTERNAL CLOCK IN USE:"
6810 PRINT "DIVIDE THE CLOCK FREQUENCY BY";Freq_int;" TO OBTAIN THE"
6820 PRINT "VSG REPETITION RATE"
6830 PRINT "MULTIPLY THE CLOCK PERIOD BY";Pulse_int+1;" TO OBTAIN THE"
6840 PRINT "PULSE LENGTH"
6850 PRINT "Time$=";Time$;"   ";
6860 PRINT "Dac$=";Dac$
6870 PRINT "  NOTE: PULSE LENGTH IS DURATION OF FINAL VOLTAGE LEVEL"
6880 RETURN     ! Exit Status
7000 Ch_f_vl: ! Enter new final voltage level, transition unchanged
7010 PRINT "PRESENT FINAL LEVEL=";Final_vl;" VOLTS"
7020 INPUT "ENTER NEW FINAL VOLTAGE LEVEL=",New_fvl
7030 Flag=0  ! Flag is set to 1 when a disallowed voltage is entered
7040 IF Tr=1 THEN GOSUB 7200 ! Calculations and error statements
7050 IF Tr=2 THEN GOSUB 7300 ! Calculations and error statements
7060 IF Flag=1 THEN 7010   ! Disallowed voltage has been entered
7070 RETURN    ! Exit Ch_f_vl
7200 Ch1_f_vl: ! Positive transition< change finalvoltage level
7210 IF Init_vl>=New_fvl THEN ! If false, valid voltage
7220 BEEP 200,.2
7230 PRINT "FINAL LEVEL <= INITIAL LEVEL NOT ALLOWED ON POSITIVE TRANSITION"
7240 Flag=1     ! Reenter final voltage level
7250 GOTO 7290  ! Execute return statement
7260 END IF     ! End of error statement
7270 Final_vl=New_fvl   ! Valid new final voltage level
7280 GOSUB 2500 ! Enter new final_vl
7290 RETURN     ! Exit Ch1_f_vl
7300 Ch2_f_fl:  ! Negative transition, change final voltage level
7310 IF Init_vl<=New_fvl THEN   ! If false, valid voltage
7320 BEEP 200,.2
7330 PRINT "FINAL LEVEL >= INITAL LEVEL NOT ALLOWED ON NEGATIVE TRANSITION"
7340 Flag=1     ! Reenter final voltage level
7350 GOTO 7390  ! Execute return statement
7360 END IF     ! End of error statement
7370 Final_vl=New_fvl  ! Valid new final voltage level
7380 GOSUB 2500  ! Enter new Final_vl
7390 RETURN      ! Exit Ch2_f_vl
7500 Ch_i_vl:    ! Change initial voltage level, transition unchanged
7510 PRINT "PRESENT INITIAL LEVEL=";Init_vl;" VOLTS"
7520 INPUT "NEW INITIAL VOLTAGE LEVEL=",New_ivl
7530 Flag=0  ! Flag is set to 1 when disallowed voltages are entered
7540 IF Tr=1 THEN GOSUB 7600
7550 IF Tr=2 THEN GOSUB 7800
7560 IF Flag=1 THEN 7510 ! Disallowed initial voltage level entered
7570 RETURN  ! Exit Ch_i_vl
7600 Ch1_i_vl: ! Positive transition< change initial level
7610 IF New_ivl>=Final_vl THEN    ! If false , valid voltage
7620 BEEP 200,.2
7630 PRINT "INITIAL VOLTAGE LEVEL>= FINAL VOLTAGE LEVEL NOT ALLOWED + TRANS."
7640 Flag=1 ! Reenter initial voltage level
7650 GOTO 7690  ! Execute return statement
```

```
7660 END IF
7670 Init_vl=New_ivl  ! Valid initial voltage level
7680  GOSUB 2500 ! Enter new initial voltage level
7690  RETURN      ! Exit Ch1_i_vl
7800 Ch2_i_vl:    ! Negative transition, change initial level
7810 IF New_ivl<=Final_vl THEN  ! If false, valid voltage
7820 BEEP 200,.2
7830 PRINT "INITIAL LEVEL<= FINAL LEVEL NOT ALLOWED ON NEGATIVE TRANSITION"
7840 Flag=1     ! Reenter initial voltage level
7850 GOTO 7890 ! Execute return statement
7860 END IF
7870 Init_vl=New_ivl  ! Valid new initial voltage level
7880 GOSUB 2500 ! Enter new Init_vl
7890 RETURN      ! Exit Ch2_i_vl
8000 Changetr:  ! Change the transition
8010 REM Final and initial levels are exchanged
8020 IF Tr=1 THEN  ! Change the transition
8030 Tr=2
8040 ELSE
8050 Tr=1
8060 END IF
8070 Exchange1=Final_vl     ! Interchange the initial
8080 Exchange2=Init_vl      ! and final voltage levels
8090 Final_vl=Exchange2
8100 Init_vl=Exchange1      ! Interchange complete
8110 GOSUB 2500  ! Enter new Tr & voltafe levels
8120 RETURN      ! End Changetr:
12155 User:! user defined routine
12160 PRINT "User"
12165 RETURN      ! Exit User
12170 END         ! End of VSG Driver
```

NUMERIC VARIABLES

C1	Control character for entering timing card functions. Contains the two least significant bits.
C2	Control character for entering timing card functions. Contains the two most significant bits.
C3=C1+C2	Hex control character for entering timing card functions.
Ck1ctrl	Decimal value of the second character of Time$, contains the clock on/clock off control bit.
Ck2ctrl	Clock control bit in Ck1ctrl is complemented, new decimal value.
Ctrl	Selects computation for DAC A or DAC B; 1= DAC A; 2= DAC B.
D	In Status routine: Length of pulse when set by delay line =(D+1)*10 nanoseconds. D is the decimal value of the hex character programmed into position 3 of Time$ to set the pulse length.
Delay_line	Length of pulse when using programmable delay line, entered by operator, range 1-16, corresponds to a range of 10-160 nanoseconds.
Exchange1	Used, with Exchange2, to interchange the initial and final voltage levels in the change transition routine.
Exchange2	Used, with Exchange1, to interchange the initial and final voltage levels in the change transition routine.
Final_vl	The value of the final voltage (Level V2 in instructions). In Trvls:, it is an entry variable.
Flag	Used in the Ch_f_vl: (Change final voltage level only) and Ch_i_vl: (Change initial voltage level only) routines Flag= 0 calculate new voltage level, Flag=1 illegal voltage level entry, reenter a new voltage level.
Freq_int	A positive integer greater then one. The internal/external clock frequency is divided by Freq_int to obtain the Vsg drive frequency. This is positions 4-7 of Time$.
Freq_int2	=65536 - Freq_int. Put in fornat for loading registers in support unit.
Init_vl	The value of the initial voltage level (Level V1 in the instructions). In Trvls:, it is an entry variable.
Lsb_s	This is the value in least significant bits of the variable Vdac+10. The entry variable Vdac in routine Code: is converted to a positive offset voltage by adding 10 to it, then digitizing it to the nearest 12 bit LSB. Lsb_s is

	then converted to the complementary offset code that is sent to the DAC registers.
New_fvl	Used in Ch_f_vl: to enter a new final voltage level. If New_fvl is a valid voltage, then Final_vl is the new final voltage level.
New_ivl	Used in Ch_i_vl: to enter a new initial voltage level. If New_ivl is a valid voltage level, then Init_vl is the new initial voltage level.
Plength	Used in Pulse_length: to enter a new value of pulse length in nanoseconds. Entered in increments of 100 nanoseconds.
Pos	Decimal value of Ck$, the hex digit in position 2 of Time$. Bit 2 of Ck$ contains the clock control bit.
Pos1	Decimal value of Pos with the clock control bit complemented to turn the clock on if off, or off if on.
Pulse_int	A positive integer less than Freq_int. The pulse length (duration of final voltage level) is equal to clock period*Pulse_int. This is in positions 8-11 of Time$. Note: Pulse_int entered from keyboard has one subtracted from it, therefore Pulse_int used in program will be one less then the keyboard entry.
Pulse_int2	=65536-Pulse_int. Put in a format to load registers in the support unit.
Raw_lsbs	Undigitized value of Lsb_s. Not used in this program.
Tr	Sets the transition. Tr=1 is positive transition (initial level to final level), Tr=2 is negative transition (final level to initial level).
Vdac	Voltage used for DAC A and B code calculations.
Vdac3	=Vdac+10. Forces voltage to be a positive number from 0 to 20 to facilitate conversion to LSB's and code calculations.
Vsg	IEEE-488 identification of the the voltage-step generator support unit. Initially set to 70812 in line 110.
Vsgfreq1	User entered Vsg drive frequency in Vsgfreq: routine. Converted to Freq_int by the relationship Freq_int=INT(10,000,000/(Vsgfreq)+0.4999999) based on the internal 10 MHz clock.
Xdacb	The output voltage, when multiplied by -0.5, needed from DAC B to produce the programmed output levels.
Xdacb1	=-0.5*Xdacb. Save if needed for later use.
Ydaca	The output voltage, when multiplied by -1, needed from DAC A to produce the programmed output levels.

Ydaca1 =(-1)*Ydaca. Save if needed for later use.

STRING VARIABLES

Bindac_a$ Set equal to X$, this is the code sent to the registers for DAC A.

Bindac_b$ Set equal to X$, this is the code sent to the registers for DAC B.

Ck$ Hex character in position 2 of Time$. Contains the clock control bit in position 2.

Ck1$ Hex character in position 2 of Time$. Used in Ckon_off: routine. Contains the clock control bit in position 2.

Ck2$ String of Ck1ctrl in binary. Bit 15 contains the clock control bit.

Ck3$ ="1"&Ck2[4]. Used to turn the clock off in line 1580. Saved for future use.

Ck_on$ Saved to turn the clock back-on, after use of Ck3$ to turn clock off.

Clear_crt$ =CHR$(255)&CHR$(75). Use, with OUTPUT 2 statement, to clear CRT screen.

Dac$ Contains the DAC coding to the support unit storage registers.
Format is "0AAABBB".
"0"=Board Address.
"AAA"=coding DAC A
"BBB"=coding DAC B

F$ Hex code for dividing the clock frequency by Freq_int. Used in Vsgfreq: routine. This is a four digit code inserted into Time$ in positions 4-7.

Hex1$ Hex string obtained from Lsb_s. The first three digits contain the coding for the 12 bit DAC's.

P$ Hex code for dividing the clock frequency by Pulse_int. Equivalent to multiplying the clock frequency by Pulse_int to find the pulse length. This is a four digit code inserted into positions 8-11 of Time$.

Time$ Contains the coding to the timing card storage registers.
Format="1GLFFFFPPPP"
"1"=Board Address
"G"=Function Select Code
"L"=Programmable delay line coding
"FFFF"=Divide the clock frequency by a four digit hex number to set the Vsg drive frequency.
"PPPP"=Divide the clock frequency by a four digit hex

number to set the duration of the final voltage level. (Pulse Length).

Tr$ ="POSITIVENEGATIVE". Substring of used in Status: routine to indicate positive or negative transition.

V$ Set equal to X$ in lines 3157 and 3210. Intermediate storage of the coding to DAC's A and B.

X$ =Hex1$[2]. After reversal of digits, contains the hex code sent to the storage registers for DAC's A and B.

Xx$ Digit two of Time$ when used in Card: routine.

Xx1$ Programmable delay line code of one hex digit inserted into position three of Time$.

LINE LABELS

Bindaca: Assemble the code for DAC A into Dac$. Ctrl=1 is used to access this routine.
Return at line 3230.

Bindacb: Assemble the code for DAC B into Dac$. Ctrl=2 is used to access this routine.
Return at 3180.

C1c2: [Key 8] Enter C1 and C2 without displaying the timing card menu. Entry variables are C1 and C2, routine can be entered at line 675 if these are set.
Return at line 700

Card: [Key 7] Display the functions available on the timing card. Variables C1 and C2 are entered to implement these functions. Can be entered at line 675 if C1 and C2 are set [no display].
Return at line 700.

Ch1_f_vl: Check positive transition, final voltage level, error statement. Lies within Ch_f_vl: routine.

Ch1_i_vl: Check positive transition, initial voltage level, error statement. Lies within Ch_i_vl: routine.

Ch2_f_vl: Check negative transition, final voltage level,error statement. Lies within Ch_f_vl routine.

Ch2_i_vl: Check negative transition, initial voltage level, error statement. Lies within Ch_i_vl routine.

Ch_f_vl: [Key 13] Change the final voltage level without changing transition or initial voltage level. Entry variable is New_fvl, when determined to be valid, Final_vl is set equal to New_fvl. Can be entered at line 7030 if New_fvl is set.
Return at 7070.

Ch_i_vl:
[Key 14]
Change the initial voltage level without changing the transition or the final voltage level. Entry variable is New_ivl, when determined to be valid, Init_vl is set equal to New_ivl. Can be entered at line 7530 if New_ivl is set. Return at 7070.

Changetr:
[Key 11]
Transition is changed, initial and final voltage levels are interchanged, and the new transition and voltage levels are output. Return at 8120.

Ck_off:
Before entering any new data to the storage registers, the clock is turned off to ensure reliable loading of the storage registers. The clock off routine turns the clock off without changing any other settings. The string Ck_on$ is used for turning the clock back on. Return at 1600.

Ckon_off:
[KEY 12]
Cycle the clock on/off or off/on. The clock control bit in Time$ is also changed to reflect the clock on/off status. Return at 770.

code:
Calculations to obtain the complementary offset binary code code to load the DAC registers using Dac$. Return at 3140.

Dac_va:
DAC A calculations for the voltage necessary to output the programmed initial and final voltage levels. Return at 3140.

Dac_vb:
DAC B calculations for the voltage necessary to out put the programmed initial and final voltage levels. Return at line 2870.

Dacv_s:
Compute and output the voltages and binary codes for DAC's A and B to obtain the programmed initial and final voltage levels using Dac$. Return at line 2640.

Delayline:
[Key 5]
Set the pulse length with the programmable delay line. Entry variable is Delay_line. Can be entered at line 6030 if Delay_line is set. Return at line 6070.

Final_vlrg:
Check the value of Final_vl to determine if a valid voltage. Lies within Trvls: routine.

Init:
[Key 0]
Set up the Voltage-step generator parameters. After executing a RUN statement, Init: must be executed. Parameters set include Tr, Dac$, Time$, Bindac_a$, Bindac_b$, Init_vl, Final_vl, Freq Int, Pulse_int and Vsg. Return at line 250.

Init_vlrg:
Check the value of Init_vl to determine if a valid voltage. Lies within Trvls: routine.

Integer: [Key 6]
Enter the pulse length and Vsg drive frequency using positive integers. Freq_int and Pulse_int are the entry variables. One is subtracted from Pulse_int entry so new Pulse_int is one less then the value entered.
Can be entered at line 5540 if Freq_int and Pulse_int are set.
Return at line 5610.

Loop:
After RUN is executed, program remains at line 90 using a GOTO Loop statement. After a key is pressed, when execution of the subroutine associated with that key is completed, the program returns to Loop:.

Neg_tr:
Sets the negative transition.
Return at line 530.

Pos_tr:
Sets the positive transition.
Return at line 510.

Pulse_length: [Key 4]
Set the pulse length based on the 10 MHz internal clock. Pulse length is entered in units of 100 nanoseconds.
Return at line 5250.

Pulse_q3:
Not used. Produces a pulse at transistor Q3 output.
Return at line 550.

Pulse_q4:
Not used. Produces a pulse at transistor Q4 output.
Return at 570.

Start:
Line 2. Not used, going to Start: equivalent to a RUN statement.
Program remains in a loop at Loop:.

Status: [Key 10]
Prints on CRT the current Voltage-step generator parameters.
Return at line 6880.

Trvls: [Key 2]
Set a new transition, new final voltage level, and a new initial voltage level. Entry variables are Tr, Final_vl and Init_vl. Can be entered at line 2060 if these three variables are already set.
Return at line 2640.

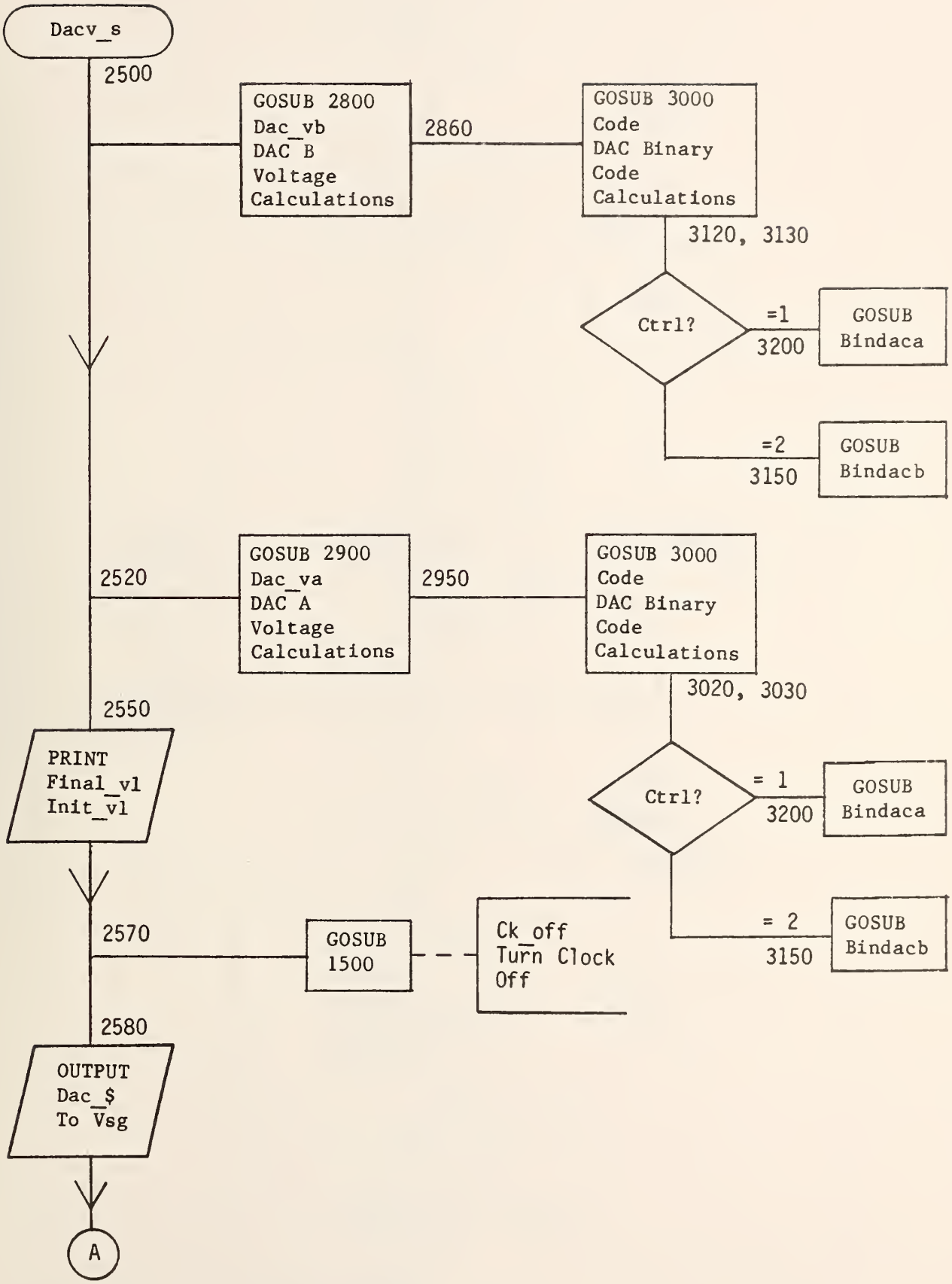
User: [Key 9]
A user defined subroutine.
Return at line 12165.

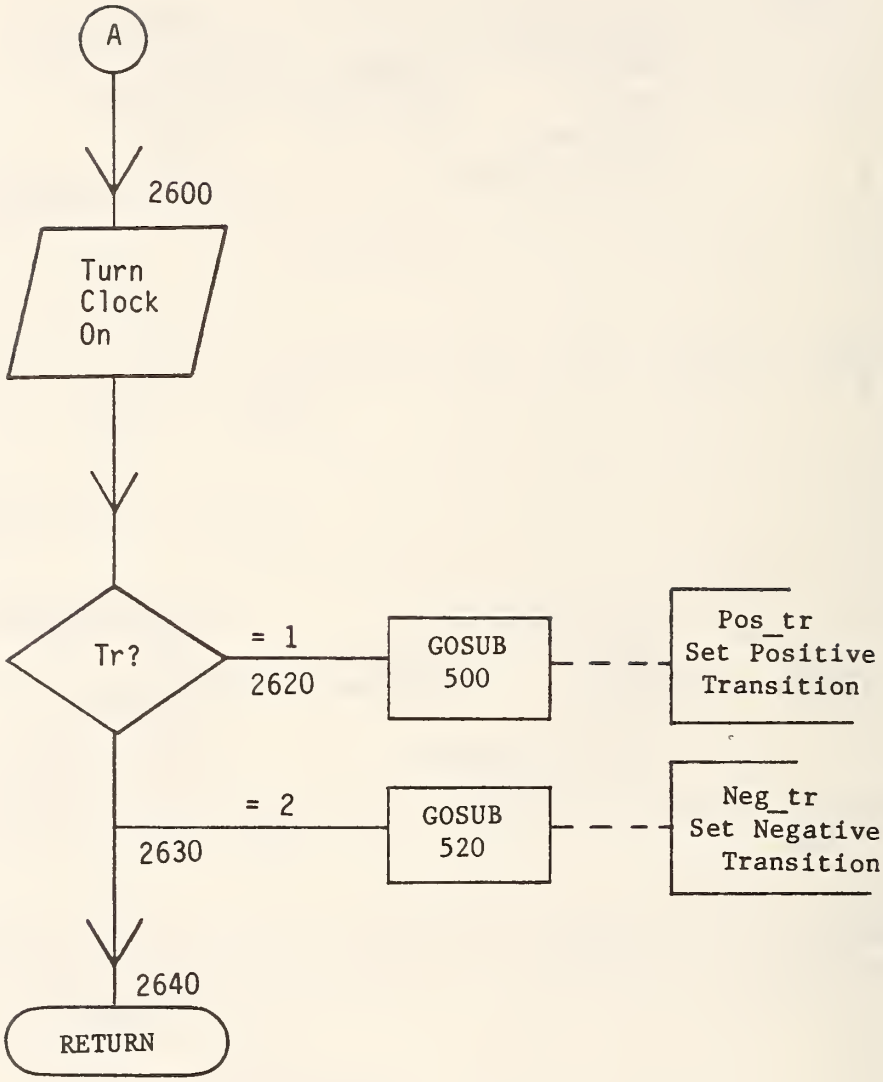
Vsgfreq: [Key 3]
Enter the Voltage-step generator drive frequency based on the 10 MHz internal clock. Entry variable is Vsgfreq1.
Can be entered at line 4040 if Vsgfreq1 is already set.
Return at line 4300.

FLOW CHARTS

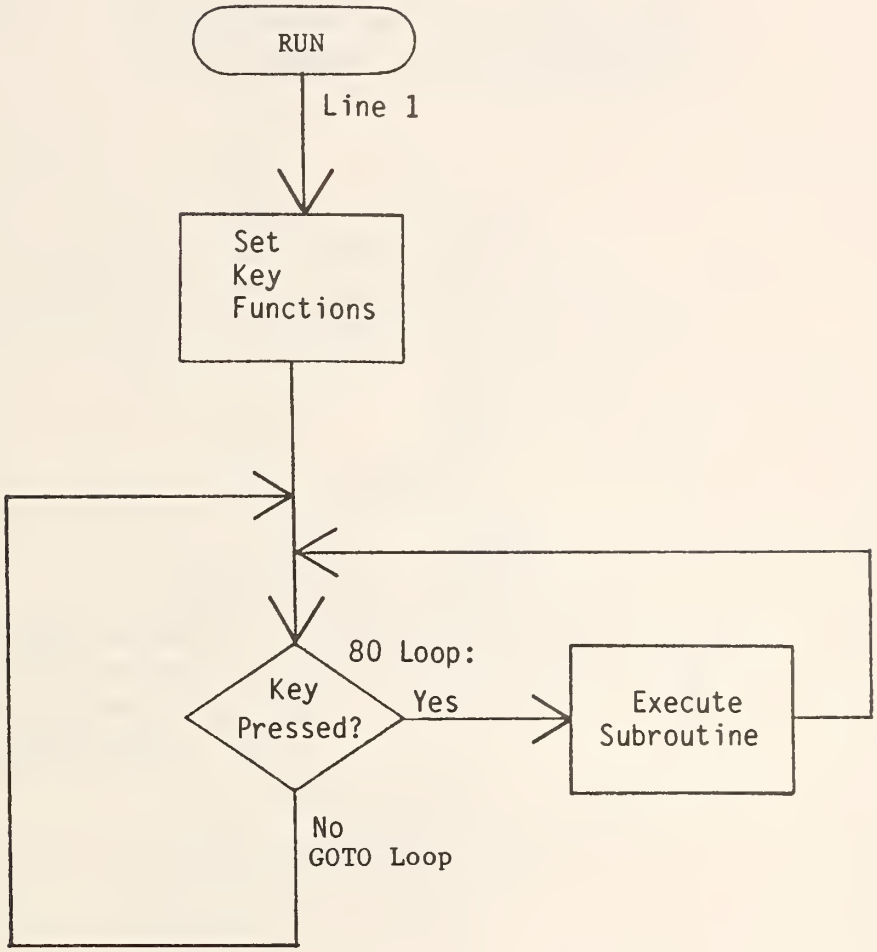
Flow charts are given for each of the defined keys and GOSUB 2500, the main routine used to calculate codes needed for the DAC's. After a RUN statement is executed , the program remains in a loop at line 80 "Loop:", and all operations are from the Softkeys.

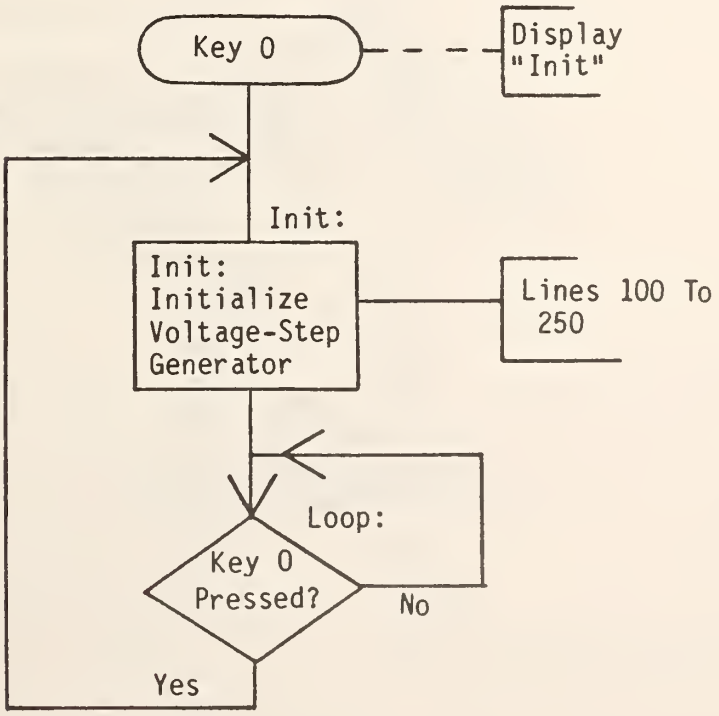
GOSUB 2500 or Dacs_s



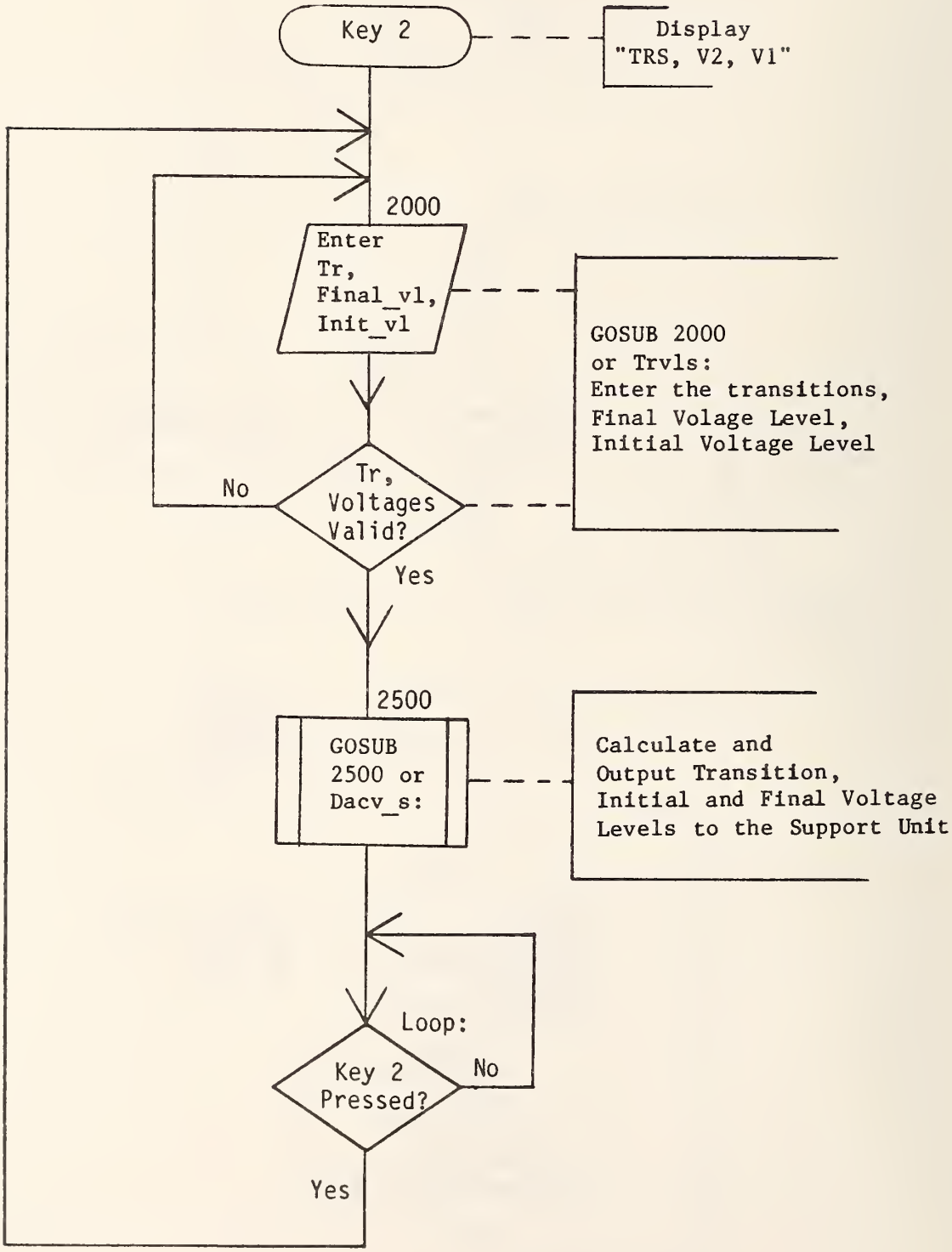

A
2600
Turn
Clock
On
Tr?
= 1
2620
GOSUB
500
Pos_tr
Set Positive
Transition
= 2
2630
GOSUB
520
Neg_tr
Set Negative
Transition
2640
RETURN

Key 0 GOSUB Init

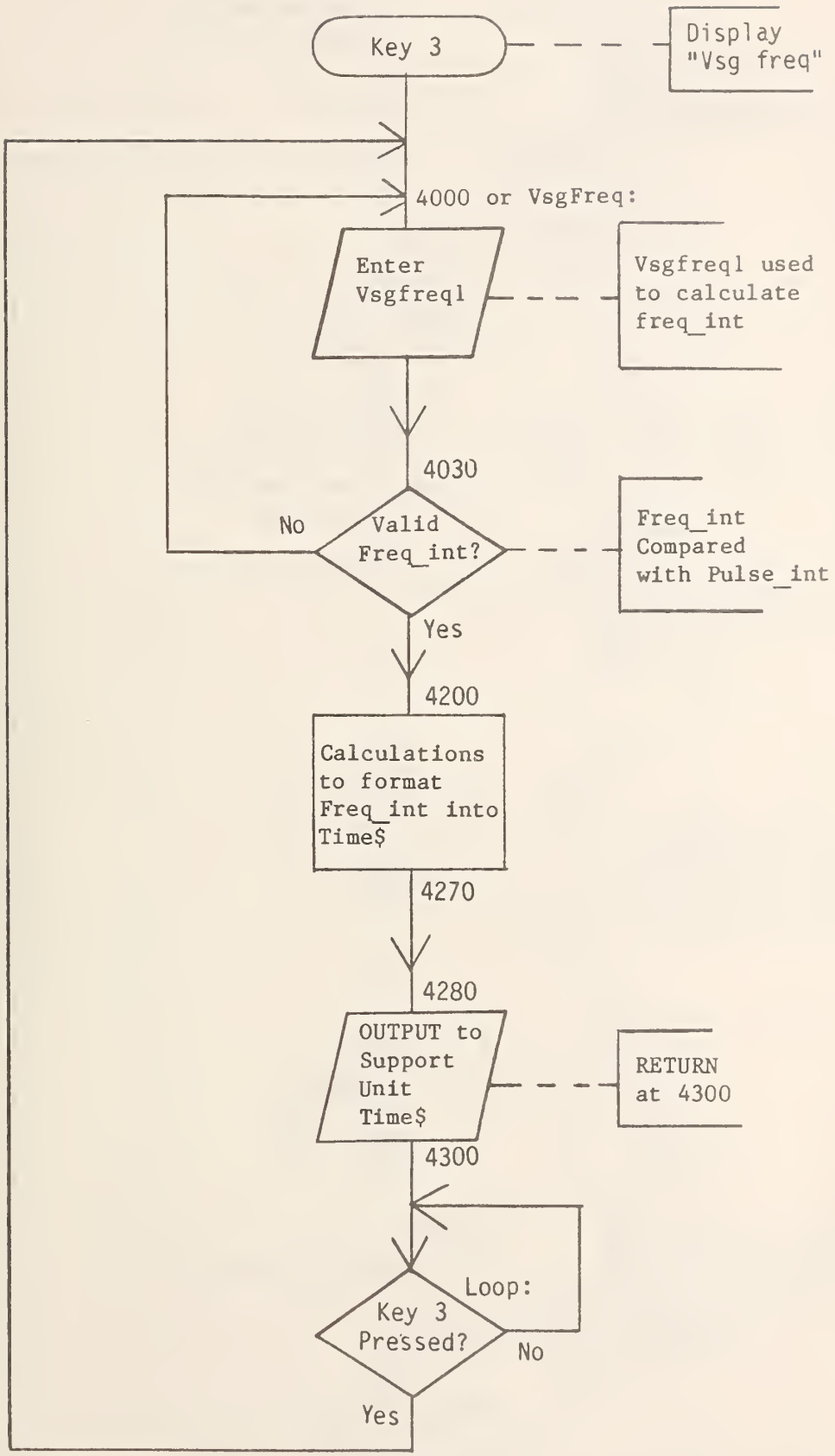




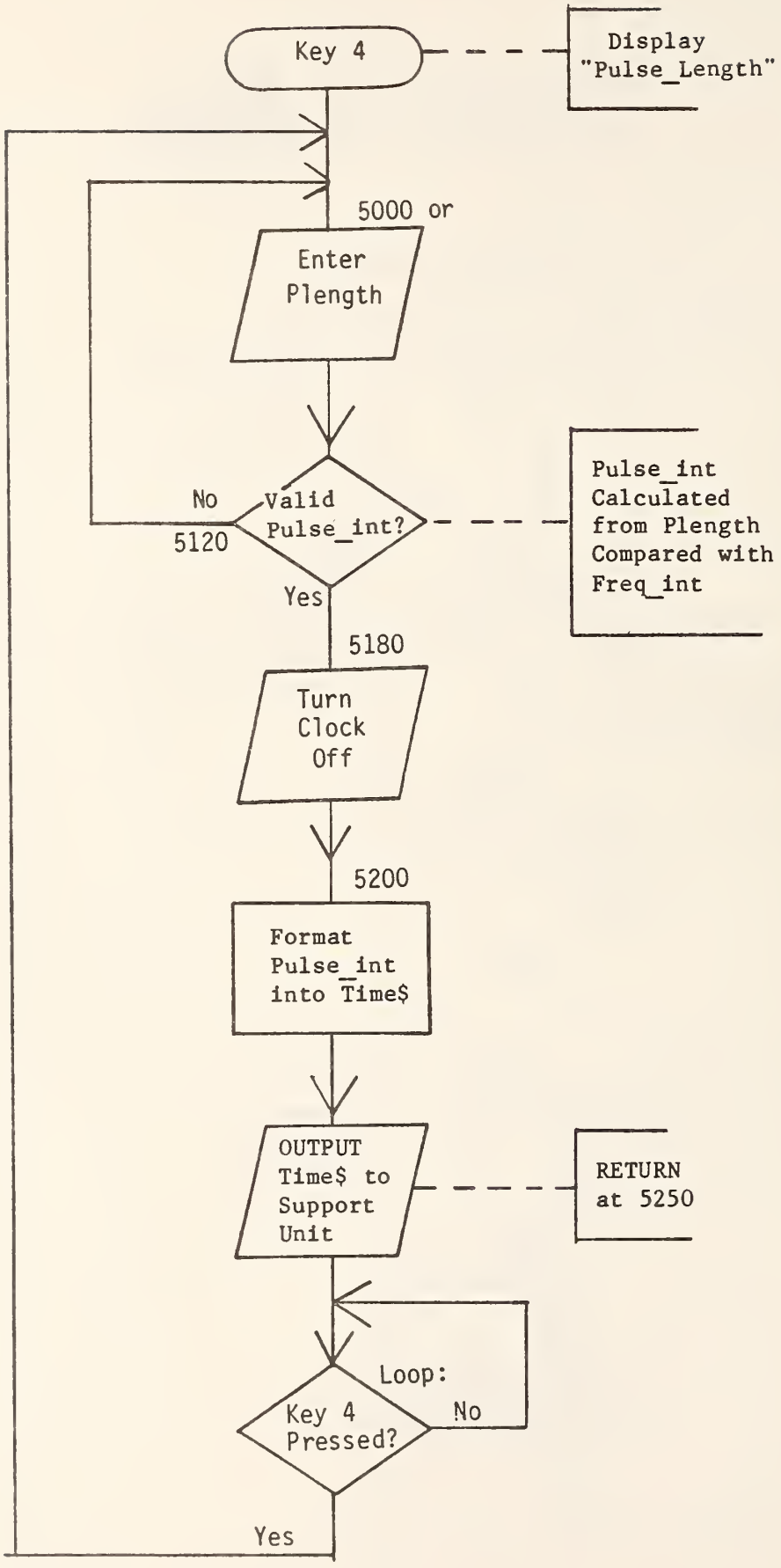
Key 2 Enter Polarity of transition,
Final and Initial Voltage Levels



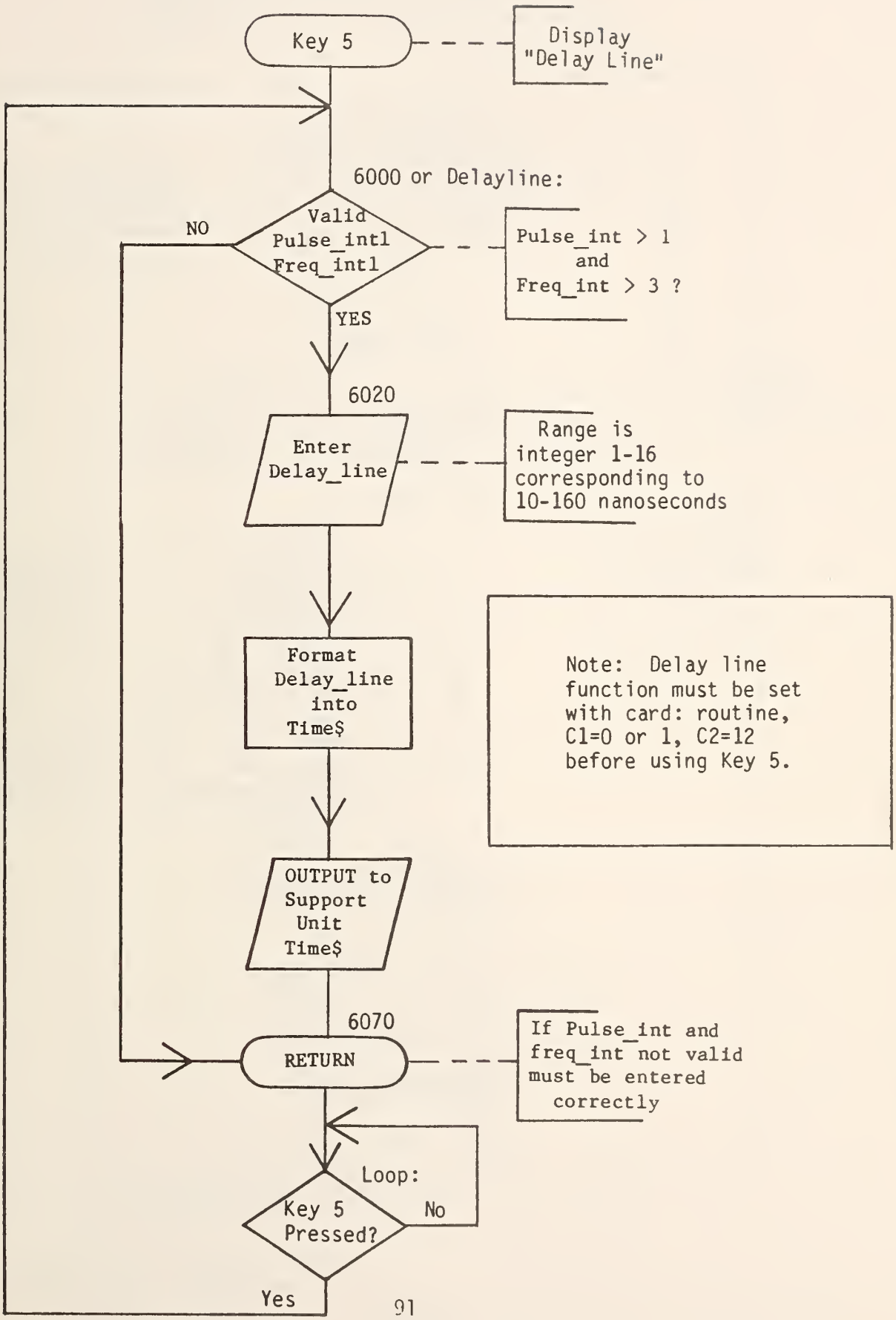
Key 3 GOSUB Vsgfreq



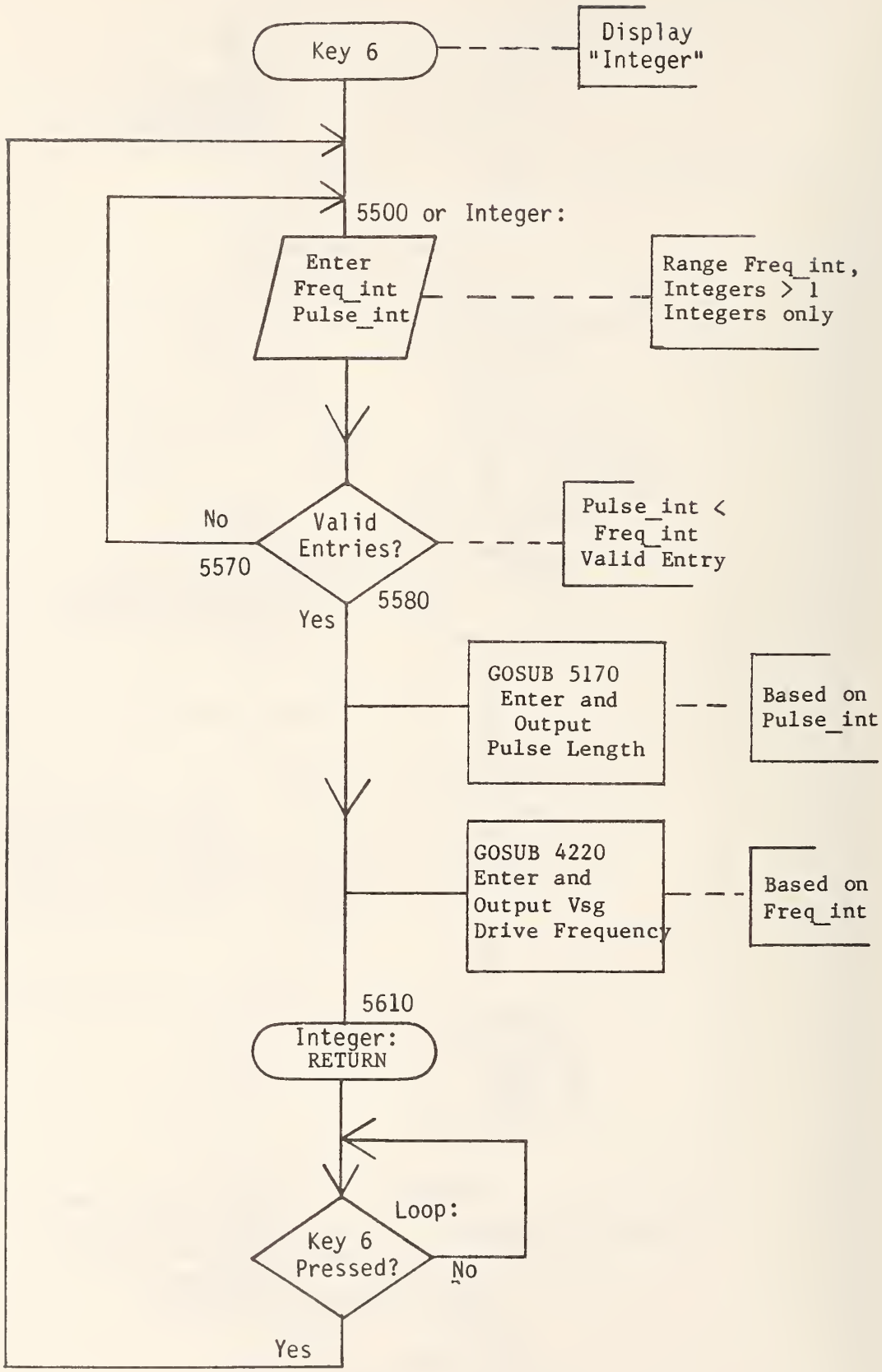
Key 4 GOSUB Pulse_Length



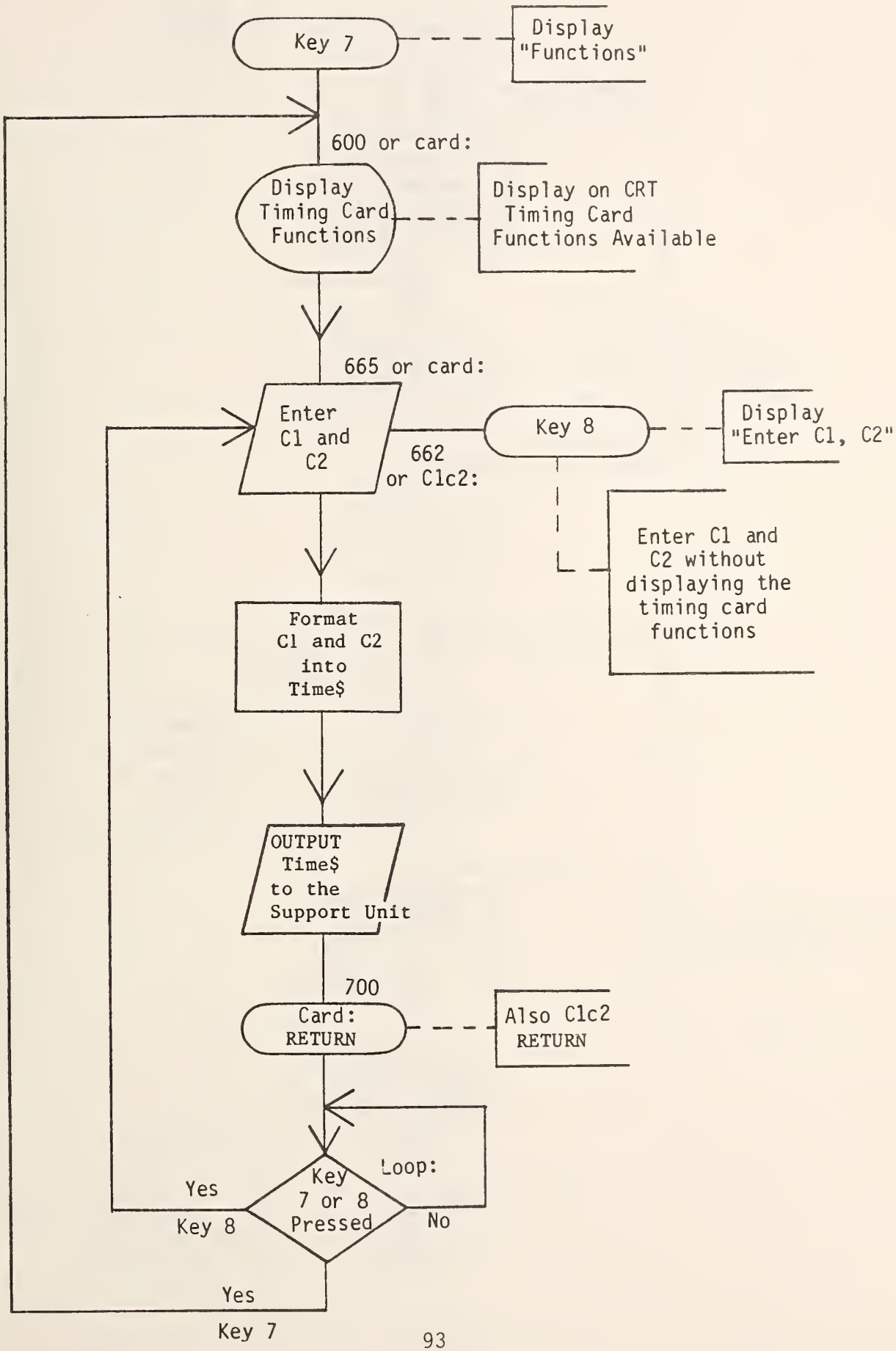
Key 5 GOSUB Delayline



Key 6 Gosub Integer

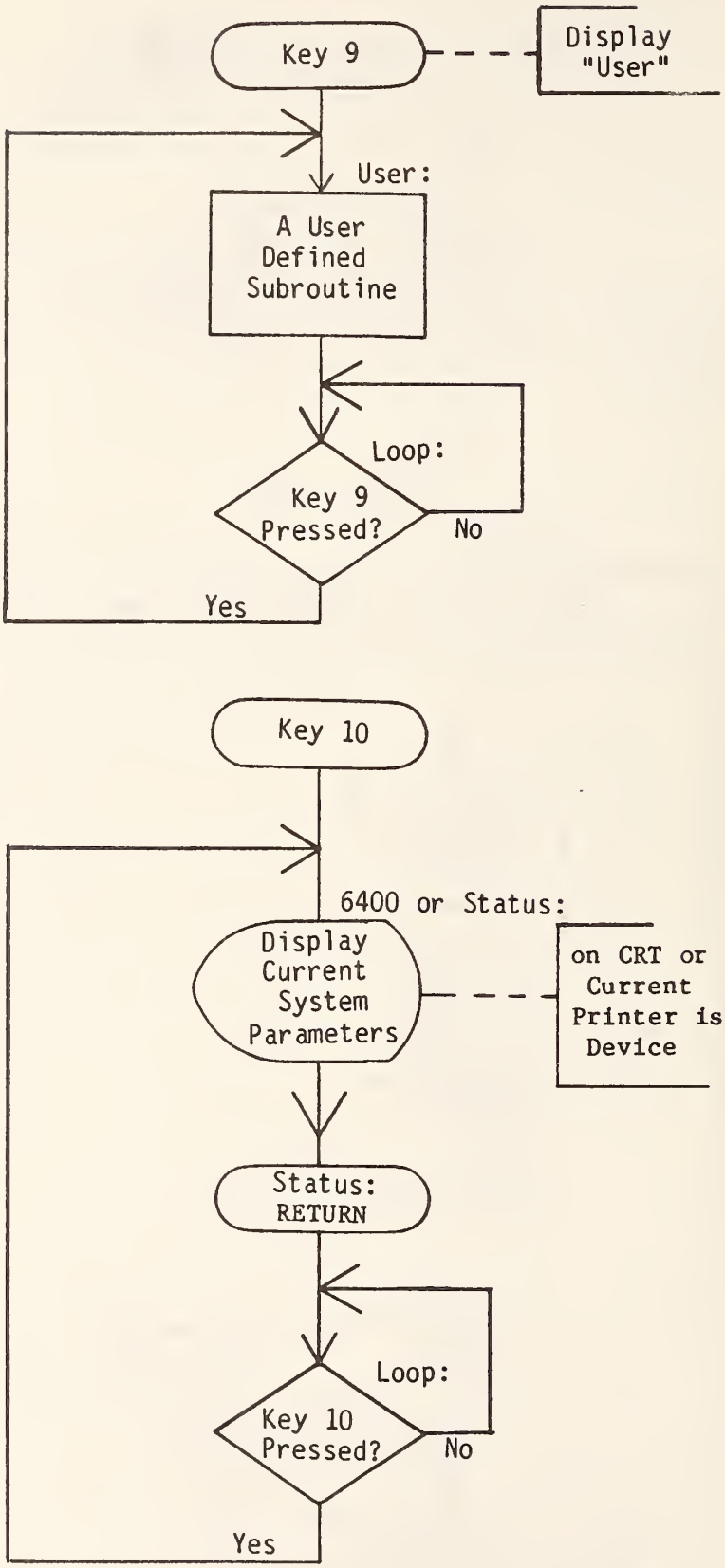


Key 7 GOSUB card
Key 8 GOSUB C1c2

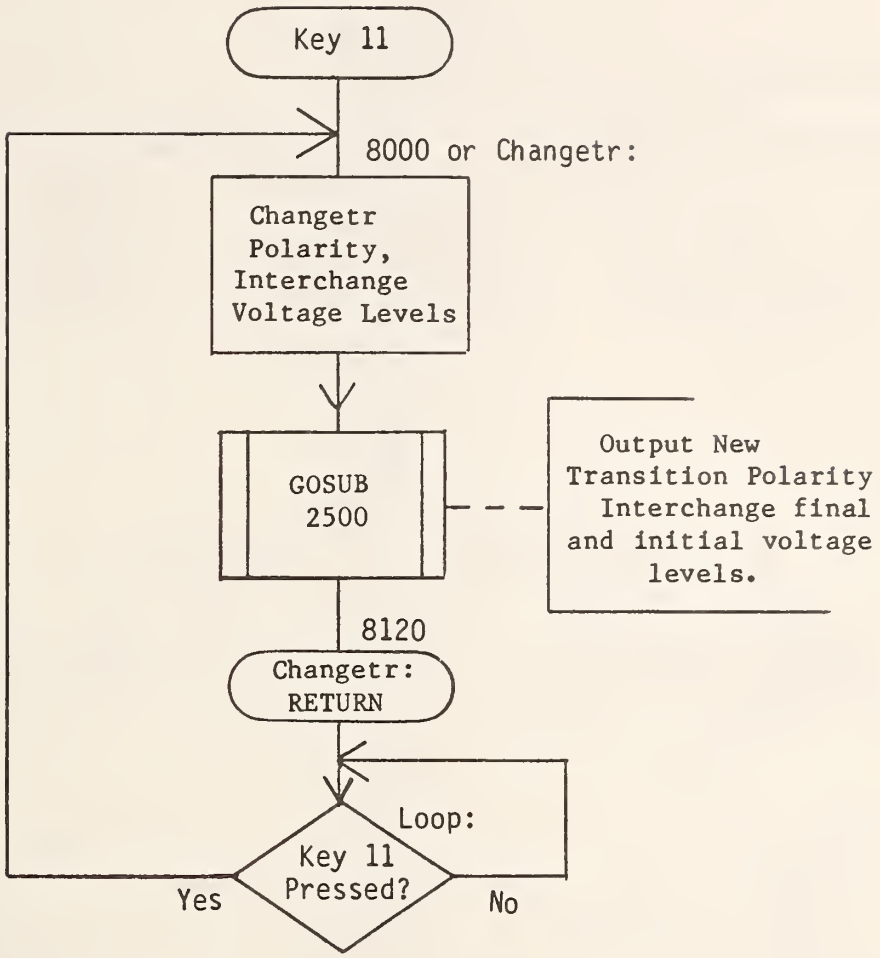


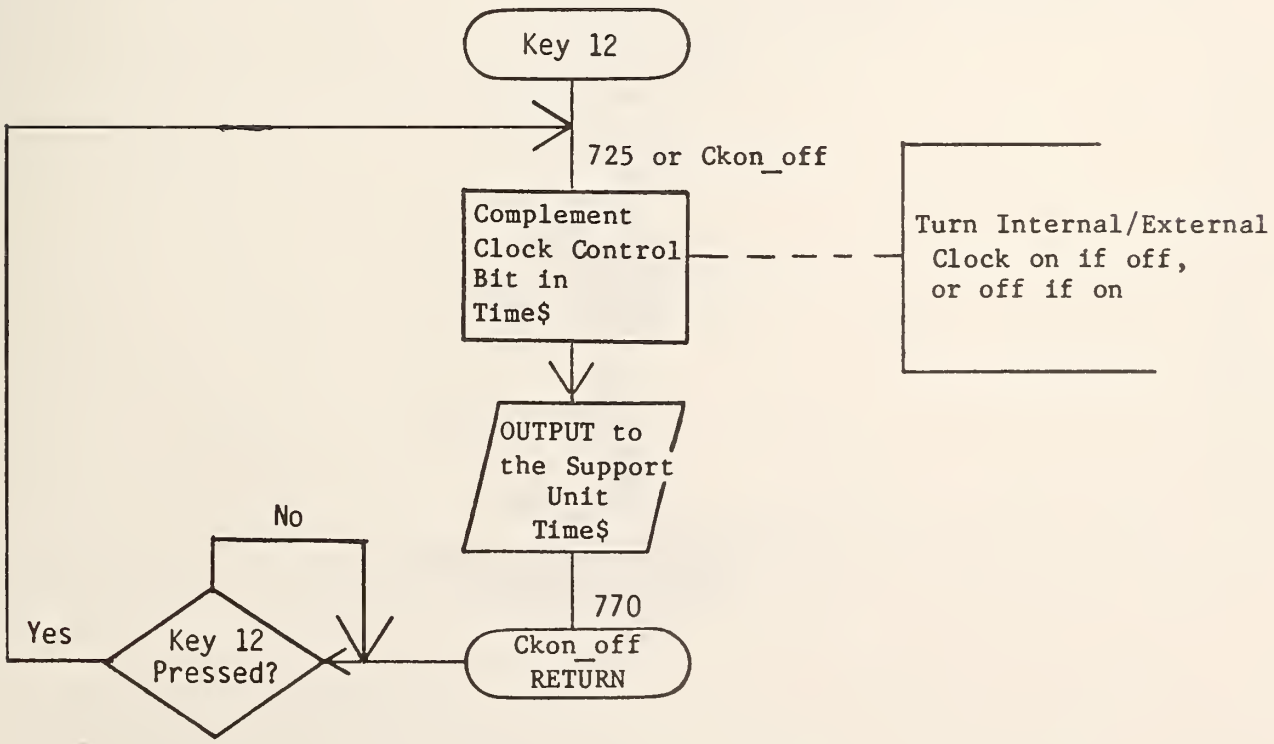
Key 9 GOSUB User

Key 10 GOSUB Status

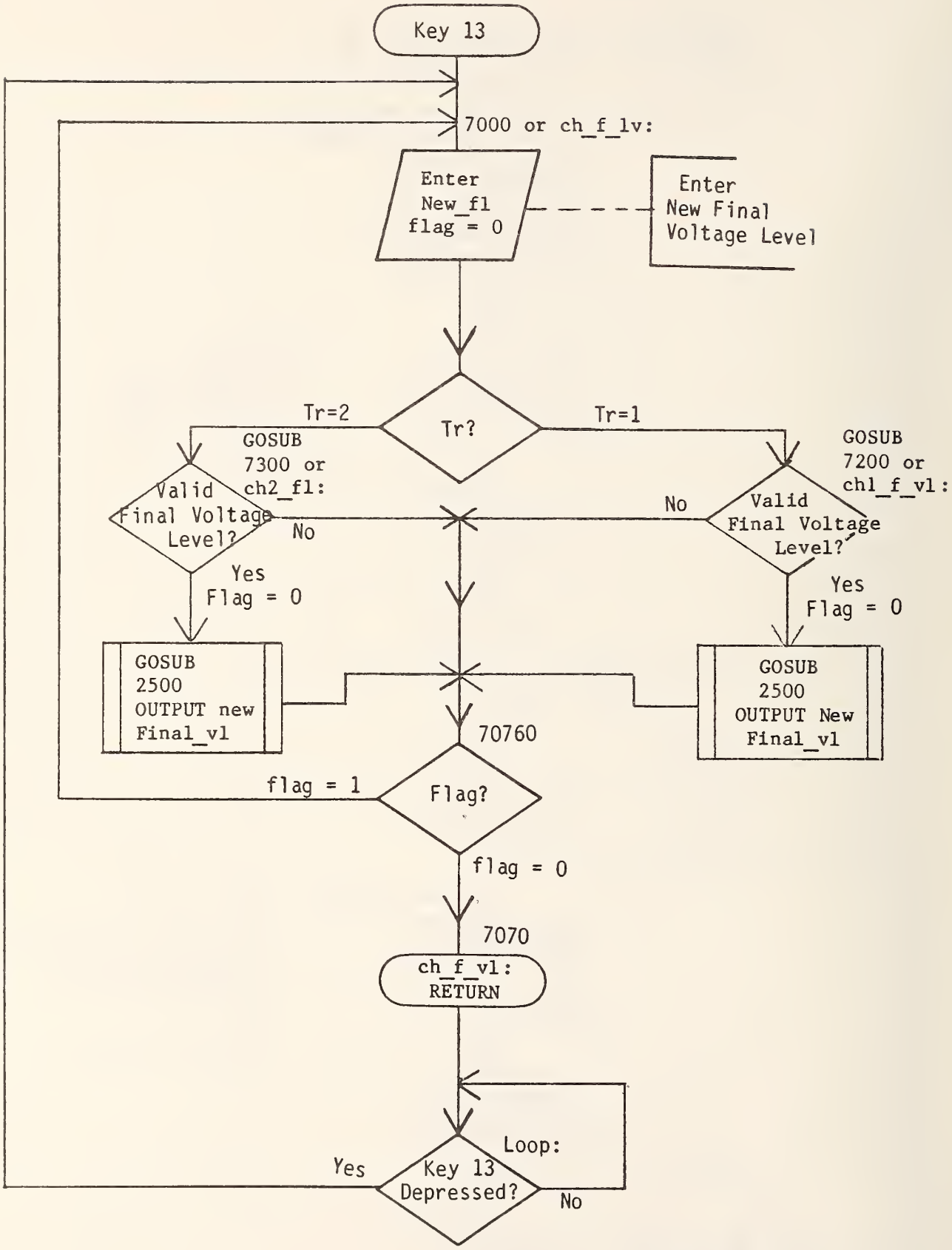


```
Key 11  GOSUB Changetr
Key 12  GOSUB Ckon_off
```

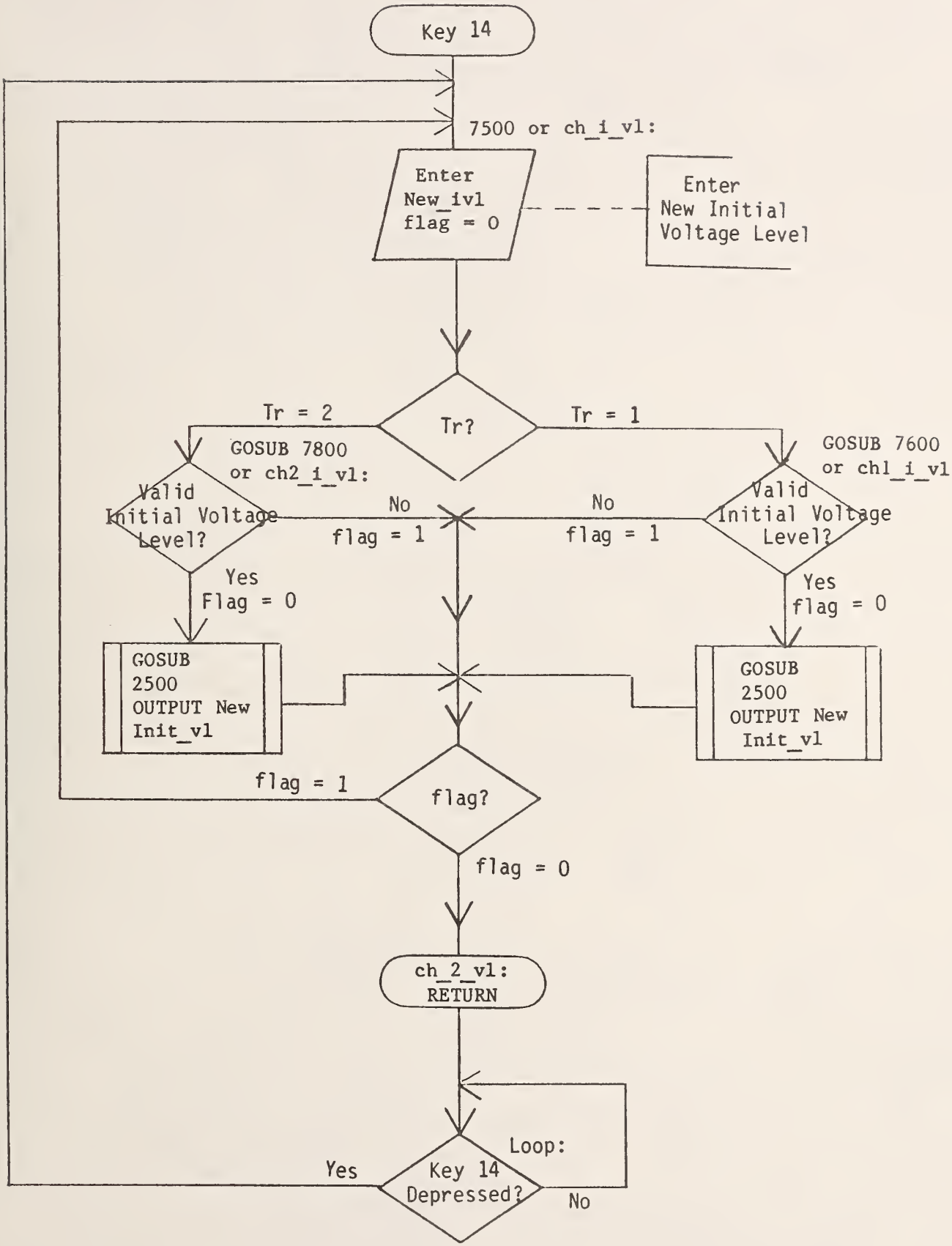




Key 13 GOSUB ch_f_vl



Key 14 GOSUB ch_i_vl



NBS-114A (REV. 2-8C)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET (See instructions)	1. PUBLICATION OR REPORT NO. NBS/TN-1230	2. Performing Organ. Report No.	3. Publication Date December 1986

4. TITLE AND SUBTITLE

A Precision Programmable Step Generator for Use in Automated Test Systems

5. AUTHOR(S)

H.K. Schoenwetter, D.R. Flach, T.M. Souders, and B.A. Bell

6. PERFORMING ORGANIZATION (If joint or other than NBS, see instructions)

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
Gaithersburg, MD 20899

7. Contract/Grant No.

8. Type of Report & Period Covered

Final

9. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS (Street, City, State, ZIP)

Same as item 6.

10. SUPPLEMENTARY NOTES

[ ] Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

A precision voltage step generator has been designed for use in automated systems to test the dynamic response of waveform recorders and other instruments. The programmable pulse parameters include transition polarity, pulse length, and repetition rate. The initial and final levels of voltage steps are each programmable within the range of ± 1 V for a 50 Ω termination and within ± 5 V for a high impedance load. Voltage steps within these ranges settle to within ± 0.02% of full scale range (FSR) in less than 22 and 26 ns, respectively, for small load capacitance. The corresponding transition durations are approximately 6 and 7 ns.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

automated test systems; programmable step generator; pulse generator; rise time; settling time; transition duration; waveform recorder testing

13. AVAILABILITY

[X] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[X] Order From Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

[ ] Order From National Technical Information Service (NTIS), Springfield, VA. 22161

14. NO. OF PRINTED PAGES

104

15. Price

NBS Technical Publications

Periodical

Journal of Research—The Journal of Research of the National Bureau of Standards reports NBS research and development in those disciplines of the physical and engineering sciences in which the Bureau is active. These include physics, chemistry, engineering, mathematics, and computer sciences. Papers cover a broad range of subjects, with major emphasis on measurement methodology and the basic technology underlying standardization. Also included from time to time are survey articles on topics closely related to the Bureau's technical and scientific programs. Issued six times a year.

Nonperiodicals

Monographs—Major contributions to the technical literature on various subjects related to the Bureau's scientific and technical activities.

Handbooks—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

Special Publications—Include proceedings of conferences sponsored by NBS, NBS annual reports, and other special publications appropriate to this grouping such as wall charts, pocket cards, and bibliographies.

Applied Mathematics Series—Mathematical tables, manuals, and studies of special interest to physicists, engineers, chemists, biologists, mathematicians, computer programmers, and others engaged in scientific and technical work.

National Standard Reference Data Series—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a worldwide program coordinated by NBS under the authority of the National Standard Data Act (Public Law 90-396). NOTE: The Journal of Physical and Chemical Reference Data (JPCRD) is published quarterly for NBS by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements are available from ACS, 1155 Sixteenth St., NW, Washington, DC 20056.

Building Science Series—Disseminates technical information developed at the Bureau on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

Technical Notes—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NBS under the sponsorship of other government agencies.

Voluntary Product Standards—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The standards establish nationally recognized requirements for products, and provide all concerned interests with a basis for common understanding of the characteristics of the products. NBS administers this program as a supplement to the activities of the private sector standardizing organizations.

Consumer Information Series—Practical information, based on NBS research and experience, covering areas of interest to the consumer. Easily understandable language and illustrations provide useful background knowledge for shopping in today's technological marketplace.

Order the **above** *NBS publications from: Superintendent of Documents, Government Printing Office, Washington, DC 20402.*

Order the **following** *NBS publications—FIPS and NBSIR's—from the National Technical Information Service, Springfield, VA 22161.*

Federal Information Processing Standards Publications (FIPS PUB)—Publications in this series collectively constitute the Federal Information Processing Standards Register. The Register serves as the official source of information in the Federal Government regarding standards issued by NBS pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations).

NBS Interagency Reports (NBSIR)—A special series of interim or final reports on work performed by NBS for outside sponsors (both government and non-government). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Service, Springfield, VA 22161, in paper copy or microfiche form.

U.S. Department of Commerce
National Bureau of Standards
Gaithersburg, MD 20899